A structure oriented compact thermal model for multiple heat source ASICs

Adam Augustin[a,*], Bartosz Maj[b], Arno Kostka[a]

[a]*Solid State Electronics Laboratory, Technical University of Darmstadt, Schlossgartestr. 8, D-64289 Darmstadt, Germany*
[b]*Continental Teves AG, Mixed Signal IC Development, P.O. Box 90 01 20, D-60441 Frankfurt, Germany*

Abstract

This paper proposes a methodology for the extraction of a compact thermal model for multiple heat source devices, which can be used for estimation of the overall temperature field. This extraction is based on the physical parameters as well as on the layout and the packaging of the device. The model directly represents the regions surrounding a source by a resistance network containing the specific parameters of source and chip in analytical form, so that it is easy to vary parameters like power dissipation and thermal conductivity within a wide range. In order to obtain a good and fast approximation of the continuous case, the shape of the volume elements represented by a node in the network is chosen regarding the direction of the heat flow within these elements. Therefore these volume elements are not rectangular but pyramid- or parallelogram-like structures. The temperature fields of multiple sources add up for the total temperature distribution, by the use of a matrix field representation.

1. Introduction

In modern complex mixed signal chips the junction temperature is not uniformly distributed across the die, but is a function of the placement of different modules in the chip layout [1–3]. The heat generating and temperature sensitive parts of the IC are therefore exposed to different temperatures, regarding their placement and power dissipation. In many devices the number of such heat generating parts can easily reach 20–30. The number of heat sensitive parts can be even bigger. Because of this fact, the specification of a single thermal resistance for characterizing such a device is not enough.

Various methods have been used to describe the thermal behavior of a semiconductor chip: numerical computation [4], e.g. Finite Element Method, or an analytic description of the temperature field, by, e.g. the image method [5,6] or the theory of the Green functions [7–9]; or a description of the entire structure of an ASIC by a network of concentrated, discrete resistances [2,10]. Often also a combination of the different methods is used [11–13].

In the method of the concentrated elements a topological resistance network is developed which mostly does not refer to the geometry of the structures, but simply describes the existence of thermal coupling within the system, in static or dynamic (including capacitors in the resistance network) case. In general it is not straightforward to find values of the network elements that give an overall good approximation. Especially the ratio of the resistances responsible for lateral or vertical flow, is difficult to obtain. In this paper the thermal response of the surroundings of a source within an ASIC will also be transferred into a resistance network, but with a closer look to the direction of the heat flow in the three-dimensional elements.

2. Model structure

Our model consists of a resistor network whose node voltages represent the temperature distribution as a function

---

* Corresponding author.

E-mail addresses: augustin@iht.tu-darmstadt.de (A. Augustin), bartosz.maj@contiteves.com (B. Maj), kostka@iht.tu-darmstadt.de (A. Kostka).

of stepwise increasing distance from the source, within a (limited) region around the source from which appreciable thermal response is to be expected.

Since the heat flow caused by a heat source on the surface of a chip runs not only perpendicularly downward, but a large part of the heat flow also spreads laterally, it is vital to describe the individual resistances in the heat flow path as well as possible. This is the reason for developing a specific geometrical model for the thermal resistance elements which is presented in Section 2.1.

The heat sources within the chip are represented by equivalent unit current sources. Their temperature response on the surface of the die is calculated from the specific thermal network. At this point, comparison with other methods (ANSYS, limiting analytical solutions) is possible. This can also be used to optimize the results by adjusting model parameters. To avoid the use of a network simulator, the voltages are computed with the help of the two-port network theory. This is possible due to the one-dimensional chain structure of the model. Voltage values determined in such a way are transferred into a unit source temperature matrix containing elements for all the points of an equidistant grid covering the chip. This matrix represents the temperature distribution for a unity source with a unity area on the surface of the die. An advantage of this normalized representation is that it contains overall scaling parameters like thermal conductivity, geometry data. Thus it is possible, with only one unit matrix, to describe different sources in different materials by simple addition, multiplication, and lateral translation operations.

2.1. Geometrical model

For the consideration of the temperature field in a solid body, a geometrical interpretation of the thermal resistance is desirable, since one can transfer the topology, i.e. the arrangement of the different layers and areas in a chip, directly to these discrete elements. Using the thermal-electrical analogon, the resistance is defined as

$$R_{\text{th}} = \frac{l}{\lambda A} \tag{1}$$

with l as length, A as cross-section area and λ as thermal conductivity of a material element with rectangular boundaries.

For our model we assume that the resistance representing the volume under the heat source, have a form similar to a frustum of pyramid. Resistances, which then border on the areas underneath the heat source, nestle themselves to those. Fig. 1 shows the resistance under the heat source with the first of adjacent pairs of resistances to its right. In [14] for a homogeneous material a propagation angle α of about 40° is suggested, without a detailed justification for this value. We will come back to this issue in Section 3.

In order to be able to adequately describe the heat flow, the volume taking part in heat conduction is described by
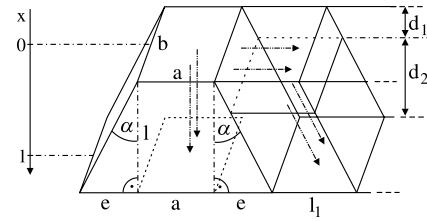

Fig. 1. Heatflow represented by three resistances.

two resistances R^{L} describing the lateral and R^{V} the vertical heat flow. Fig. 2 shows such a thermal network.

The heat conducting volume is divided around the source into n disk/layers, which are represented by n pairs of chains. Because of symmetry only one half of the chain is needed. It should be noted that the resistance chain has to be long enough so that a current flow at the chains end can be set to zero, which means that there is no remarkable thermal effect further away from the source.

We investigated two cases of source geometry: an infinite line and a (small) square.

2.2. Infinite line source

For a line source regarded as infinite in one direction, the isotherms spread parallel to the source. In other words, if one cuts in a plane perpendicular to the heat source, then the temperature distribution looks always alike, no matter in which place of the material, along the source, the cut is placed.

For the temperature distribution the resistance R_0 in Fig. 2 plays a special role. It describes the entire volume directly underneath the heat source. For the heat flow under the heat source, one can assume that the heat conducting area increases with the increasing distance from the source. In order to take this into account, the resistance R_0 is calculated in dependence of the opening angle α. For a source with the surface $A_0 = ab$ the angle-dependent resistance R_0, in accordance with Fig. 1, becomes

$$R_0 = \frac{1}{\lambda} \int_0^l \frac{1}{Kx + L} \, dx \tag{2}$$

with $K = 2b \tan(\alpha)$ and $L = ab$. According to [15] this integral is always analytically solvable, independent of whether the source surface shape is rectangular or a square. The integral represents a sum of infinitesimally thin layers,
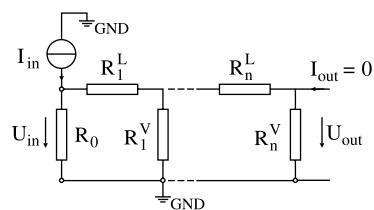

Fig. 2. Heat flow represented by a resistance chain.