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A new rule-based clustering technique for defect analysis

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Abstract

In joining defects on semiconductor wafer maps into clusters, it is common for defects caused by different sources to overlap. Simple morphological image processing tends to join either too many unrelated defects together or not enough together. Expert semiconductor fabrication engineers have demonstrated that they can easily group clusters of defects from a common manufacturing problem source into a single signature. Capturing this thought the process of clustering is ideally suited for rule-based systems. A system of rules was developed to join disconnected clusters based on the location of the defects. The clusters are evaluated on a pair-wise basis using the rules and are joined or not joined based on a threshold. The system continuously re-evaluates the clusters under consideration as the rules change with each joining action. The techniques used to measure the features, and methods for improving the speed of the system are developed. Examples of the process are shown using real-world semiconductor wafer maps obtained from chip manufacturers.
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Keywords: Rule-based; Defect clustering; Semiconductor inspection; Manufacturing

1. Introduction

Optical inspection of semiconductor wafers has long been the primary means of detecting the sources of wafer defects. Semiconductor yield engineers use high-resolution images of individual defects to assess problems in the manufacturing process. Since high-resolution off-line defect review is time consuming and expensive, process engineers also use low-resolution images of the spatial distribution of the defects (or 'spatial signatures') to identify the problem source (or 'event'). These low-resolution images are called wafer maps. Often engineers cannot determine these problems until several wafers have been inspected. Even when these spatial signatures do not contain significant portions of 'killer defects', they provide a window into the manufacturing process that can be invaluable towards quickly identifying equipment problems.

In the majority of semiconductor assembly, the visual inspection process of wafer surfaces depends on manual review by human experts. Since the inspection task requires extreme concentration, the time that an inspector can continue the task is quite limited, and still, it tends to be quite slow and inaccurate. The decision instability of an inspector can be quite large against various defect classes, and each inspector relies on different features and strategies [1]. Also the increasing demands for miniaturization, high electrical performance and high I/O pin count have resulted in intensive research and development of advanced IC (integrated circuit) packages [2,3], which results in much critical inspection task.

Once wafer map objects have been grouped into high-level sets, descriptive feature measurements are incorporated into a higher resolution classification paradigm that relates a particular spatial signature with a specific manufacturing problem [4]. A key component of the advanced clustering techniques that step beyond common proximity-based clustering methods has been discussed [5], which utilizes a gravitational force analogy to connect clusters together. Another technique employed to cluster groups of defects is fuzzy logic.

Simple morphological image processing tends to join either too many unrelated defects together or not enough together. Expert semiconductor fabrication engineers have demonstrated that they can easily group clusters of defects from a common manufacturing problem source into a single

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signature. Capturing this thought the process of clustering is ideally suited for fuzzy logic. A system of rules was developed to join disconnected clusters based on the location of defect clusters.

The clusters are evaluated on a pair-wise basis using the rules and are joined or not joined based on a threshold. The system continuously re-evaluates the clusters under consideration as their rules change with each joining action. The techniques used to measure the features, and methods for improving the speed of the system are developed. Examples of the process are shown using real-world semiconductor wafer maps obtained from chip manufacturers. The superior clustering offered through rule-based systems enables more accurate feature measurements and process characterization for the classification process.

2. Background of development

There are many reasons for poor quality of die surface, which arises due to defects on the die surface. These defects are categorized as follows.

2.1. Foreign material

It is defined as any particle on the surface of the die that bridges two unpassivated metallization or bridging active metallization to scribe line. Fig. 1 shows the image of a foreign particle on a die surface.

2.2. Discolored die pads

Fig. 2 shows an evidence of dark or discolored die pads on wafer die pads.

2.3. Bridging defect

Fig. 3 shows an evidence of bridging two distinct aluminum areas.

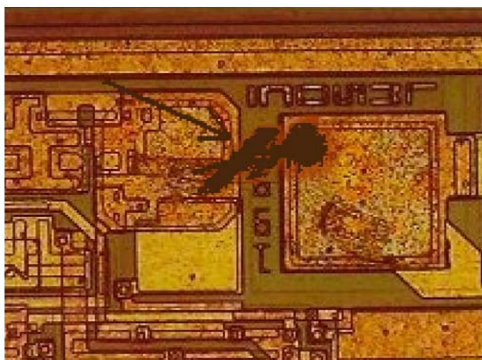

Fig. 1. Foreign material on a die surface.

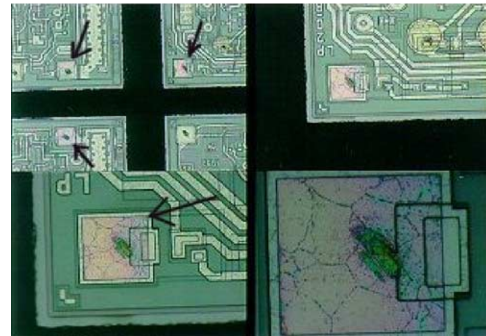

Fig. 2. Image of defective dark die pads.

2.4. Metallization defect

Fig. 4 shows an evidence of etched out aluminum metal on bond pad area.

2.5. Chip out defect

Fig. 5 shows an evidence of chip outs extending into the active regions of the die affecting an Equi-Potential Ring (EQR) when present.

2.6. Scratches

Fig. 6 shows an evidence of scratch on the die surface.

The amount of data generated in extracting all these defect features is high. Processing all this information

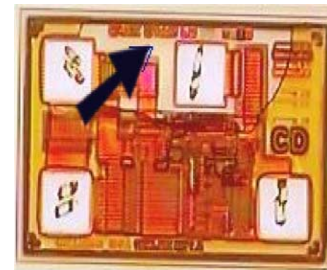

Fig. 3. Image of bridging defect.

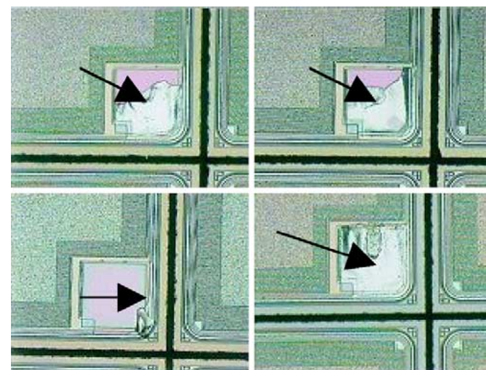

Fig. 4. Image of etched out metal on bond pad area.

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