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Switched-current (SI) integrators with reduced effect of transistor mismatches

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Abstract

Switched-current (SI) circuits are widely used for analog sampled-data signal processing, due to their compatibility to the pure digital CMOS process. As their main building blocks are current mirrors, they suffer from the effects of MOS transistor parameters mismatch. In this paper, the Functional Block Diagram (FBD) of already known integrator circuits is modified in such a way that the number of required current mirrors is reduced. Thus, the behavior of the derived integrator topologies, with respect to the effect of MOS transistor parameters mismatch, is improved.

A comparison is performed, concerning the performance of the proposed bilinear integrator circuits and those that are already introduced in the literature. For this purpose, a fifth-order Chebyshev lowpass SI filter transfer function was simulated. In the case of the proposed filter configurations, the obtained results show that their performance is improved in terms of the effects of MOS transistor parameters mismatch, DC power dissipation, and total required silicon area.
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1. Introduction

The switched-current (SI) technique has been introduced in order to overcome the requirement for CMOS process with two polysilicon layers available, which is the preferred one in the case of switched-capacitor (SC) filters. As a result, SI technique is fully compatible to the pure digital CMOS process. Also, due to the current-mode nature of SI circuits, they offer suitability for high-frequency applications and potential for low-voltage operation [1–4].

On the other hand, one of their major error sources is the mismatch of MOS transistor parameters of threshold voltage (V_T), current factor ($\beta = \mu_o C_{ox} W/L$), and channel-length modulation factor (λ). This causes DC offset current, AC linear gain error, and harmonic distortion (HD) at their output [3,4]. Other error sources are the clock-feedthrough (CFT) effect and finite transconductance-output conductance ratio of MOS transistors. A significant number of papers have been published in the literature, in order to cancel or minimize these effects. As a general conclusion, the S^3I technique seems to be a high-performance solution for this purpose [5–11].

In this paper the study is focused on the effect of MOS transistor parameters mismatch. Initially, a family of SI circuits has been introduced in the literature, where the basic memory cell realized using a current mirror [1,2]. These circuits, called '*first generation SI circuits*', were not suitable for designing filters with a clock frequency much higher than the filter cut-off frequency, or with a high *Q*-factor. The above restrictions are the result of their high sensitivity to MOS transistor parameters mismatch. As an alternative approach, the '*second generation SI circuits*' were introduced [12,13]. In this case, the basic memory cell has been realized using a current-copier circuit. Their main advantage, in comparison to the '*first generation SI circuits*', is that a lower sensitivity to MOS transistor parameters mismatch is achieved.

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As in the case of SC filters, SI integrators are very useful building blocks for realizing high-order SI filters. Integrators can be used for functionally simulating the LC ladder prototypes (Leapfrog-type SI filters), or for realizing high-order transfer functions using second-order blocks (SI biquads) [2–4,11]. Leapfrog-type LDI SI filters are very attractive due to the simplicity of their structure, as they constructed from loops formed by Forward and Backward-Euler SI integrators. On the other hand, a drawback is that the LC ladder terminations cannot be exactly simulated and, thus, a frequency depended error is occurred. In order to cancel the resulted inaccuracy, similar techniques to those proposed in the case of SC filters should be applied [14,15].

In Leapfrog-type bilinear SI filters the simulation of termination loops is accurately achieved. Thus, SI bilinear integrator circuits are very useful building blocks for simulating the operation of LC ladder prototypes. In this case, the only occurred restriction is the well-known Nyquist theorem. Bilinear SI integrators can be implemented: (a) as the sum of output currents of a Forward-Euler and a Backward-Euler integrators [16], and (b) using two current copier cells in a loop configuration and appropriate additional circuitry [11]. In order to reduce the number of required current mirrors, fully differential/balanced structures have been proposed. These give an increased bandwidth and significantly improved immunity to common-mode noise, in comparison to that offered by the corresponding single-ended structures. The price paid for the aforementioned improvements is that the circuit complexity is increased [17–19].

In this paper, single-ended inverting Forward-Euler and Bilinear SI integrator circuits are presented. The realization of the proposed blocks was done in such a way that the number of required current mirrors is reduced, in comparison to the configurations that are already introduced in the literature. This is achieved after a manipulation of the required delays and inversions in the integrators' FBD, in order to eliminate the terms which should be realized using current mirrors. In Section 2, Forward-Euler SI integrator circuits, with and without resistive damping, are presented. In Section 3, SI bilinear integrator blocks are introduced. For comparison purposes, a fifth-order Chebyshev lowpass discrete-time transfer function was simulated in Section 4. This has been done by using the proposed and the corresponding already known bilinear integrator circuits. The obtained results show that the modified filter topologies have better performance with respect to the effect of MOS transistor parameters mismatch. In addition, their DC power consumption and total silicon area are reduced.

2. SI Forward-Euler integrators

2.1. Proposed SI integrator cells

The FBD and a circuit of inverting Forward-Euler SI integrator are depicted in Fig. 1. These are based on [13],

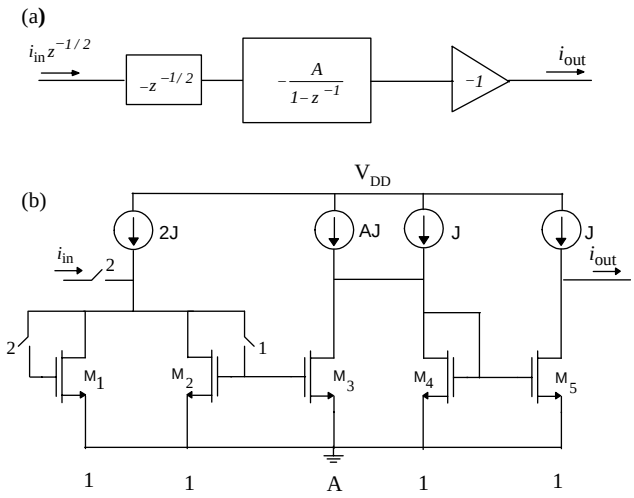

Fig. 1. SI Forward-Euler inverting integrator [13]. (a) The corresponding FBD. (b) Configuration using an extra current mirror.

with an extra current mirror employed in order to realizing the required current inversion. The transfer function of the circuit in Fig. 1b is

$$H_{1/1}(z) = \frac{i_{out}(z)}{i_{in}(z)} = -\frac{Az^{-1}}{1-z^{-1}} \quad (1)$$

Note that the general notation $H_{i/j}$ is used for the transfer function, where i and j represent the corresponding time slots in which sampling of input and output currents occurs.

From Fig. 1 it is concluded that term $(-z^{-1})$ is realized using the current copier cell, formed by transistor M_1. The scaling factor $(-A)$ is realized using two current mirrors, formed by transistors M_2–M_3 and M_4–M_5, in a cascade connection.

According to the Fig. 1a, the numerator $N(z)$ of the transfer function is formed as the following product

$$N(z) = (-z^{-1}) \times (-A) \times (-1) \quad (2)$$

The proposed modification of the above FBD is based on an alternative expression of the numerator in Eq. (1). The total delay and the simple (without delay) inversions are properly shared within the intermediate stages, in order to minimize the number of required current mirrors. Thus, the proposed form of Eq. (2) is:

$$N(z) = (-z^{-1/2}) \times (-z^{-1/2}) \times (-A) \quad (3)$$

From Eq. (3) it is concluded that only one current-mirror is required, in order to realize the scaling factor $(-A)$. The terms $(-z^{-1/2})$ in the above expression, could be easily implemented using current-copier cells. The modified FBD and the corresponding circuit of Forward-Euler integrator are shown in Fig. 2a and b, respectively.

The analysis of the circuit in Fig. 2b is based on the assumption that that both input and output of the circuit are sampled at time slot 1 of each sampling period. At time

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