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A novel ultra-high compliance, high output impedance low power very accurate high performance current mirror

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ABSTRACT

In this paper a novel ultra-high compliance, low power, very accurate and high output impedance current mirror/source is proposed. Deliberately composed elements and a good combination (for a mutual auto control action) of negative and positive feedbacks in the proposed circuit made it unique in gathering ultra-high compliances, high output impedance and high accuracy ever demanded merits. The principle of operation of this unique structure is discussed, its most important formulas are derived and its outstanding performance is verified by HSPICE simulation in TSMC 0.18 μm CMOS, BSIM3 and Level49 technology. Simulation results with 1 V power supply and 8 μA input current show an input and output minimum voltages of 0.058 and 0.055 V, respectively, which interestingly provide the highest yet reported compliances for current mirrors implemented by regular CMOS technology. Besides an input resistance of 13.3 Ω, an extremely high output resistance of 34.3 GΩ and −3 dB cutoff frequency of 210 MHz are achieved for the proposed circuit while it consumes only 42.5 μW and its current transfer error (at bias point) is the excellent value of 0.02%.

1. Introduction

Current mirrors are one of the essential widely used building blocks in analog integrated circuits. They are used to perform current amplification, biasing, active loading and level shifting. Hence, their efficient design improves the overall performance of the system. The most important parameters of current mirrors are accuracy, input/output compliances, input/output impedances, frequency bandwidth, linearity, noise and sensitivity to changes in load impedance. In many high performance applications, the performance of the simple current mirror is inadequate, especially due to low output resistance and high current transfer error. The traditional method to increase the output impedance and improve the accuracy is using cascode transistors to (equalize drain–source voltages of mirror transistors and) reduce channel length modulation effect. However cascoding the transistors increases the required supply voltage and decreases input/output compliances, which is not compatible with today's technology trend. Due to technology down scaling and its intrinsic benefits, the trend in VLSI design is to reduce voltage supply. Hence, low voltage and low power circuit designs are in great demand. It can be found that there are many researches dealing with methods to improve the performance of low voltage current mirrors. Some of these methods are based on using level shifters [1,2], FGMOS transistors [3,4] and bulk driven schemes [5–7]. Although these methods operate with low power supplies and maintain high compliances, but unfortunately they suffer from some drawbacks. Two first solutions introduce extra offset to the output current. Offset can be canceled using adaptive biasing, but at the cost of increasing power consumption and extra circuit complexity. FGMOS transistors suffer from charge entrapment during fabrication process, large capacitance DC biasing and special technology that requires higher design cost comparing to traditional transistors [8–10]. Moreover, they are not suitable for DC processing. Bulk driven current mirrors also suffer from current offset problem, low bandwidth, high power consumption and limitations imposed by implementation process [6].

One of most widely used current mirrors is the low voltage cascode one. It has moderately low input and high output impedances, moderately low input and output voltages and high accuracy. To further decrease its input voltage and impedance, the input current can be applied to the drain of the transistor M_1 [11] (Fig. 1a). However this method introduces some offset to the output current. This offset current can be eliminated by subtracting it from the input or the output node. However it increases the circuit's complexity and requires much more attention in the design of biasing network. The better solution is obtained using an amplifier to equalize the drain–source voltages of mirror transistors. The other advantage of this solution is that it also improves other specifications of current mirror such as input and output impedances. This method is implemented in [12–14]. In [12] in order to

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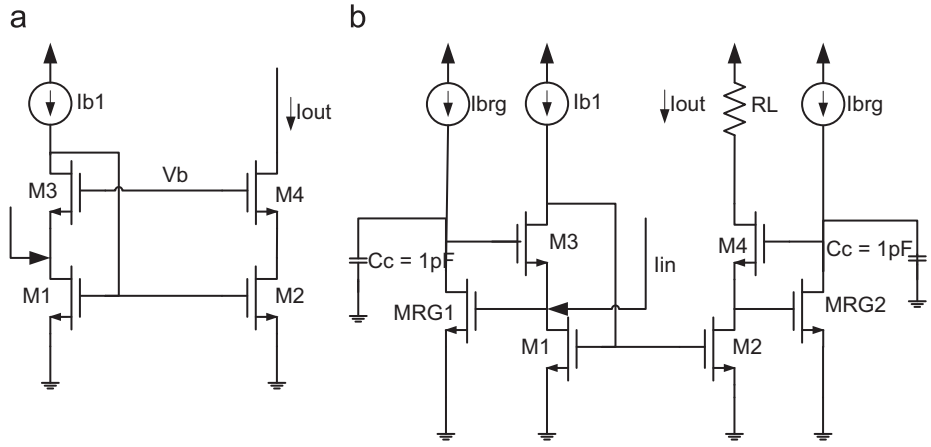

Fig. 1. (a) Low Voltage Cascode Current Mirror (LVCCM) and (b) regulated version of (a).

maintain M_{A1} and M_{A2} transistors in saturation mode of operation, V_{GS} of transistors M_{1C} and M_{2C} must be less than the threshold voltage of M_{A1} and M_{A2}. This may not be possible in some CMOS technologies. Careful designing of biasing network is required in [13] and circuit proposed in [14] uses floating gate transistors in its feedback loop, when its limitations were notified earlier. Moreover, all these circuits [12–14] suffer from complexity and their compliances are relatively low. Some recently reported simple and low voltage circuits are discussed in [15–17] in which their structures are as simple as low voltage cascode current mirror but their performance are inadequate in some applications where high output and low input impedances are needed [15].

In this work a novel high performance current mirror is presented that improves most of the aforementioned features acceptably. Simple structure of this current mirror gives a relatively high bandwidth and low power consumption. Its compliances are the highest yet reported for circuits implemented with regular CMOS technology, while exhibiting extremely low input and extremely high output impedance. Current dynamic range of the proposed current mirror is larger than that of low voltage cascode current mirror while maintaining a very high accuracy.

In Section 2 the proposed high performance current mirror is explained. Section 3 includes the HSPICE simulation results using TSMC 0.18 μm, BSIM3, Level49, CMOS technology and finally Section 4 concludes the paper.

2. Proposed high performance current mirror

2.1. Principle of operation

The proposed current mirror, conceptual schematic shown in Fig. 2, consists of a high swing cascode current mirror (M_1–M_4, with M_4 transistor connected as diode), M_5 as output transistor and an amplifier with gain amplitude of "$-A$". The high swing cascode is biased with $I_{b1}=I_{b2}=I_b$ currents and its input impedance is reduced using an FVF block [18] at input node and is driven by the input current signal I_{in}. Both cascode transistors M_3 and M_4 experience the same bias current; hence V_{ds1} is set equal to V_{ds2}, prohibiting the channel length modulation effect and thus a very high accurate result is attained. M_4, the diode connected cascode transistor, makes a separate biasing voltage source unnecessary. This transistor, on the other hand, provides the input and output nodes with an extra positive feedback loop, which increases the performance of the block without using extra circuitry. This structure includes two nested feedback loops in the input side. One of them is a negative shunt feedback implemented with an FVF

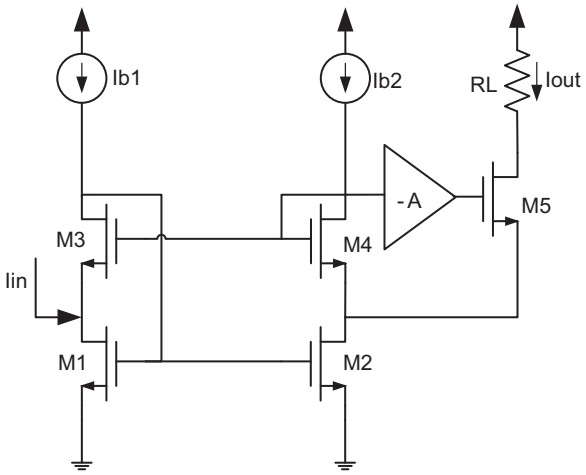

Fig. 2. Conceptual schematic of the proposed current mirror.

while the other one is a positive series type consisting of transistors M_1–M_4. Both loops act simultaneously and are specially devised to reduce the minimum input voltage, $v_{in,min}$, and the input impedance. Similarly, the output side includes two feedback loops, one of them is a negative series implemented by transistors M_4–M_5 and amplifier of "$-A$" and the next one is a positive shunt feedback consisting of transistors M_1–M_4. These two loops act simultaneously and are specially arranged to reduce the minimum output voltage, $v_{out,min}$, and increase the output impedance. In conventional method a negative series feedback is used to increase the output impedance. This reduces the output compliance by at least $1V_{dsat}$. In other word the feedback acts while the output voltage is greater than $2V_{dsat}$. By further decreasing the output voltage the feedback gain falls rapidly, causing the output impedance to be decreased rapidly due to the transistors entering the triode region.

Based on conventional definitions, MOS transistor linear region occurs when its output voltage becomes lower than $1V_{DS,sat}=V_{GS}-V_{GS,off}$ (i.e. $V_{DS}<V_{GS}-V_{GS,off}$), which leads to sharp reduction in output current versus voltage reduction. In other words for a transistor with constant V_{GS} voltage, the channel length modulation causes significant reduction in transistor output resistance. This means that I_{DS} becomes very sensitive to variation in V_{DS} in this region.

According to $I_{DS}=\beta(V_{GS}-V_{TH})^2(1+\lambda V_{DS})$, the transistor current, I_{DS}, can be varied by both V_{GS} and V_{DS}. When transistor output voltage approaches to negative supply (here ground), then V_{DS} will