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Temperature, humidity, and bias acceleration model for a GaAs pHEMT process

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ABSTRACT

This paper investigates the moisture failure acceleration factors for a GaAs pHEMT process. The activation energy Ea and the moisture accelerating factor *n* were extracted and were shown to be different from those previously reported for Si devices and for another GaAs pHEMT process. The impact of bias was studied and a humidity-induced semiconductor failure model, incorporating bias acceleration, was proposed.

1. Introduction

Temperature, humidity, and bias testing (THB) and Highly Accelerated Temperature and Humidity Stress Testing (HAST) are used interchangeably to qualify semiconductor products for operation in uncontrolled environments. The two tests are considered equivalent for silicon products using aluminum metallization. It is not immediately evident, however, that the two tests would produce equivalent results for compound semiconductor products. Quite different activation energy and moisture acceleration factor were extracted for a GaAs pHEMT process by Ersland et al. [1] in comparison to those for silicon devices [2]. This result is not unexpected. Since the acceleration factors are related to the physical mechanism of degradation, and since the materials used in compound semiconductor devices differ from those used in silicon devices, it is expected that the moisture accelerating factors would differ as well.

The purpose of this study was to verify the validity of the moisture acceleration model presented in [2] for a 0.15 μm gate length GaAs pHEMT process used in commercial applications, to extract the moisture acceleration factors for the process, and to establish appropriate moisture-test conditions for qualification of products using this process.

2. Materials and methods

Accelerated moisture testing was performed on a converter MMIC built on a GaAs pHEMT process which utilizes transistors with 0.15 μm Ti/Pt/Au gates, a dual-recess FET channel, Ni/Ge/Au ohmics, SiN MIM capacitors, TaN thin-film resistors, a three-layer metal interconnect, and an SiN passivation.

Twenty die per wafer, from two different wafers built in two different processing lots were tested at each test condition. A best attempt was made to use die covering the entire wafer for each test. The moisture acceleration factors were extracted independently for each wafer in order to establish their repeatability within the process.

The MMICs were assembled into open-cavity ceramic pin-grid-array (PGA) packages for moisture testing. Open-cavity testing with solder die-attach was chosen in order to avoid potential complications from the package materials, such as package delamination, corrosion of the package components, and silver dendrites. These package-related failure mechanisms could cloud the results and make it more difficult to evaluate the moisture failure mechanisms at the die level. Devices were prescreened after assembly using a visual inspection and a pinch-off test.

Individual failure times were recorded during testing. The failure criterion was a catastrophic short. Since intermittent shorts were observed over the course of the testing for most samples, failure time was recorded at the first occurrence of a short for each sample. Series resistors at the gate and drain bias for each MMIC limited the current through the fai`led devices, allowing for physical failure analysis to be performed post test. Each leg of the experiment was run to a minimum of 80 % cumulative failure. Results were fit with a log-normal distribution.

3. Results

Eleven life-tests were conducted using different ambient temperature, relative humidity, Vgs and Vds bias. All tests were conducted

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Table 1
Test matrix used for establishing *Ea* and moisture acceleration factor *n*.

85 °C, 85 % *RH*	110 °C, 85 % *RH*	130 °C, 70 % *RH* 130 °C, 77 % *RH* 130 °C, 85 % *RH* 130 °C, 95 % *RH*	150 °C, 85 % *RH*

Table 2
Test matrix used for establishing voltage acceleration factor *m*.

Vgs = −2 V, Vds = 5 V	Vgs = −3 V, Vds = 6 V Vgs = −2 V, Vds = 6 V Vgs = −1.5 V, Vds = 6 V	Vgs = −2 V, Vds = 7 V

under pinched conditions (no power dissipation). A total of 220,000 device-hours of life-testing were accumulated on the project.

3.1. Temperature and humidity acceleration

According to the existing model [2], device life time under elevated humidity and temperature can be described as

$$t = \frac{A}{RH^n} e^{\frac{Ea}{kT}}, \tag{1}$$

where t is life time, A is a constant, RH is relative humidity, n is the moisture acceleration factor, Ea is the activation energy, k is Boltzmann's constant, and T is absolute temperature.

A test matrix was designed (Table 1) to validate the applicability of the above model to the pHEMT process under consideration, and to extract the activation energy and moisture acceleration factor. Bias was kept constant for those tests: Vgs = −2 V and Vds = 6 V. Probability plots of the data are shown in Fig. 1.

From this test matrix, we extracted

Wafer 1: $Ea = 0.63$ eV, $n = 8.7$,

Wafer 2: $Ea = 0.60$ eV, $n = 7.3$.

The extracted moisture activation parameters for the two wafers were found to be consistent with each other within confidence level bounds, thus, signifying a single moisture failure mechanism exists for the process. It is worth noting that the extracted activation energy is slightly lower while the moisture acceleration factor is quite higher, compared to those for aluminum corrosion in silicon devices ($Ea = 0.77$–0.81 eV, $n = 2.5$–3 [2]). Additionally, the activation energy extracted in this study is quite lower than the activation energy for another GaAs pHEMT process ($Ea = 1.7$ eV, $n = 10.7$ [1]), while the moisture acceleration factor is slightly lower. This shows that the same moisture acceleration factors do not apply to all compound semiconductor devices. Therefore, a best practice would be that the moisture acceleration factors are extracted for each unique technology in order to make proper life time predictions based on accelerated moisture testing.

3.2. Impact of bias on life times

The impact of bias on life time was also studied. The test matrix used was such, that different Vgs, Vds, and Vgd bias conditions were applied, while keeping the FETs pinched (Table 2). All testing was performed at 130 °C and 85 % relative humidity.

A surprising bias dependence of life time was observed. Life times were found to be independent of Vds within the small voltage range studied. However, a strong dependence of Vgs was seen. Probability plots of the data from the voltage studies are shown in Fig. 2.

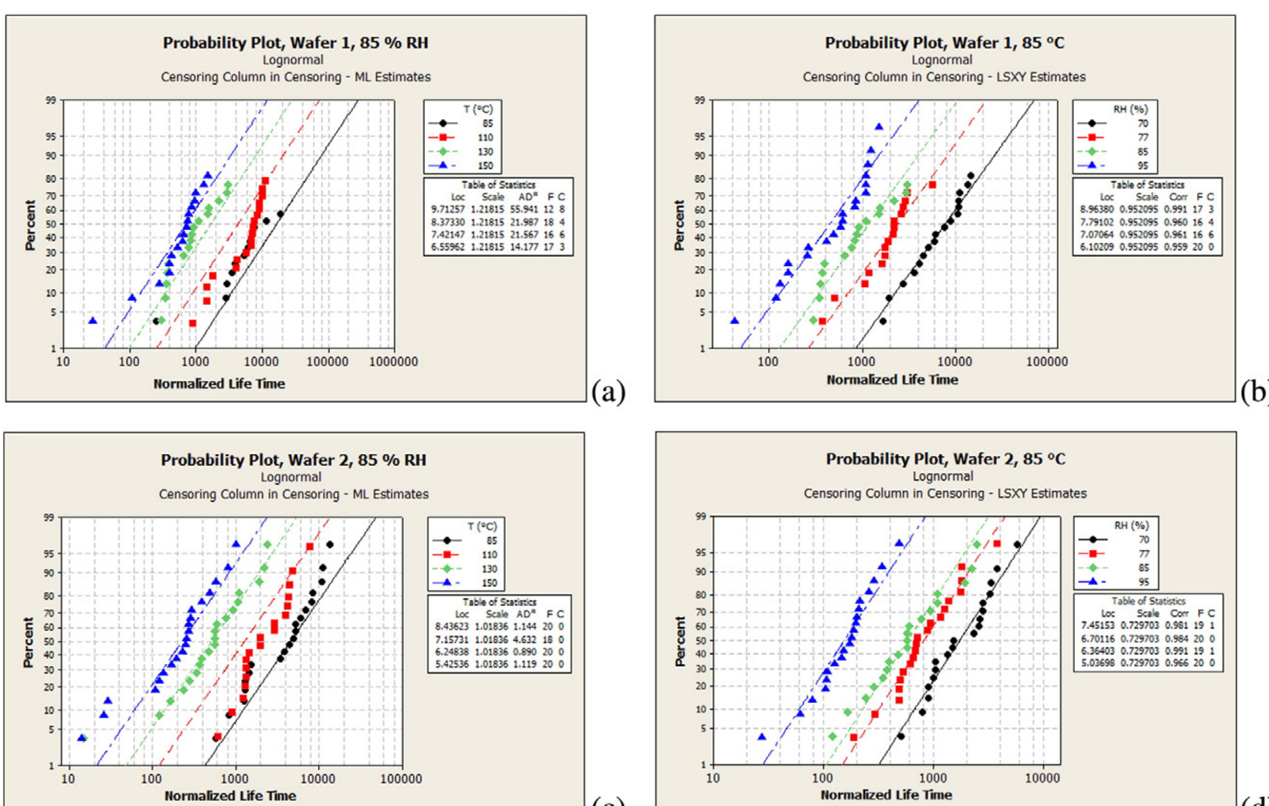

Fig. 1. Probability plots of normalized life times at Vgs = −2 V and Vds = 6 V for wafer 1 (a) and (b) and wafer 2 (c) and (d) used for extracting the moisture-induced failure activation factors *Ea* and *n*.