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Design and process related MIM cap reliability improvement

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ABSTRACT

A root cause failure investigation was performed on anomalous (early) MIM capacitor failures on an HBT MMIC process. These failures were only observed on capacitors in the actual MMICs; process control monitor (PCM) capacitors were nominal. Multiple failure analysis techniques were employed to determine the most probable root cause of the early failures. The root cause was determined to be etching of the capacitor dielectric by a chemical used in the MMIC fabrication process, at a step after the capacitors themselves were fully built. It was determined that only CAD layouts with certain features were susceptible to the etching. These features were not present on the PCM capacitors.

A design based corrective action was recommended to eliminate the failure mechanism. The effectiveness of the corrective actions was verified with several designed processing experiments. These experiments also demonstrated that the failure rate of the faulty parts increased with the time (even if the parts were not in operation). Finally, the experiments showed that the reliability of a nominal capacitor with a BCB layer on top was better than that of an identical capacitor without the BCB layer.

Capacitor reliability model: For the sake of completeness, the following discussion on ramped voltage TDDB testing of capacitors is included. In this work, ramped voltage data was not used to predict capacitor lifetimes, but it was used to quantitatively compare capacitor reliability by plotting percent cumulative failure versus failure voltage.

Normally, destructive ramped voltage testing and the linear field model are employed in order to estimate the lifetime of capacitors.

This method has been described in detail elsewhere for intrinsic capacitors (Cramer et al. [1,2,3]). It is generally assumed that defects on or in the capacitor bottom plate or in dielectric itself causes a localized thinning of the dielectric which shortens the intrinsic lifetime of the capacitor, as illustrated in Fig. 2.

Extrinsic capacitors require a refinement of the Nominal Thickness Method to the Effective Thickness Method. Typically, plots of percent cumulative failure versus failure voltage will be transformed into plots of percent cumulative failure versus lifetime via the above equations. The shapes of these two plots are nearly identical, only the values on the abscissa are changed from (linear) voltage to (logarithmic) lifetime. Since, in this work, the effort was directed at root cause determination of anomalous failures rather than predictions of expected lifetimes, the linear field model was never employed and the data was always plotted as a function of failure voltage.

1. Introduction

An investigation was conducted into early life capacitor failures which had been reported on GaAs HBT MMICs. These failures were only observed on capacitors in the actual MMICs; process control monitor (PCM) capacitors were nominal. In some cases, these MMICs had been packaged and integrated into the next level of assembly when the failures occurred. The fact that the MMICs had passed on-wafer screening and failed at a later time complicated the root cause investigation. Furthermore, failures were reported as having occurred across a wide range of times, from as little as after 2 h of testing up to after 100 h, making a pinpoint diagnosis of when the failures occurred difficult (Figs. 1–3).

Initial optical inspection of the failed capacitors indicated that all shared common signatures, such as visible edge defects and the melting of the capacitor bias feeds. These feeds were metal layers on top of a BCB layer, which is a feature of the NGES HBT MMIC process. An example which typifies the failures is shown in Fig. 4.

Once it was known that these capacitor failures had occurred, on-wafer MMIC data was re-evaluated with an eye toward any MMIC which failed to pass RF and DC screening criteria. Visual inspection of these MMICs indicated that some of those failures could be attributed to the same capacitor failures which had already been observed in packaged parts. Thus the span of time for failures was extended to include instantaneous failures in addition to those already described.

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Linear (Constant Voltage) Field Lifetime Model

$$t \propto \exp[-\gamma(E)]$$

Transformation of Ramped-Voltage to Constant Voltage

$$t = t(o) * \exp[\gamma([E_R - E])]$$

t time to fail at the operating voltage
γ linear field acceleration factor
E_R field at the ramped voltage failure
E field at the operating voltage
t(o) effective time constant

$$t(o) = \frac{\Delta \tau}{1 - e^{-\gamma \Delta E}}$$

Δτ ramp step time
ΔE ramp step field

Fig. 1. The linear field model.

Linear Field Equation

$$t(F) = t(0)\exp[\gamma(E_F - E_A)]$$

Nominal Thickness Method

$$t(F) = t(0)\exp[\gamma(\frac{V_F}{h} - \frac{V_A}{h})]$$

$$t(0) = \frac{\Delta t}{1-\exp(-\gamma \Delta E)} = \frac{\Delta t}{1-\exp(-\gamma \frac{\Delta V}{h})}$$

Effective Thickness Method

$$t(F) = t(0)\exp[\gamma(\frac{V_F}{heff} - \frac{V_A}{heff})]$$

$$t(0) = \frac{\Delta t}{1-\exp(-\gamma \Delta E)} = \frac{\Delta t}{1-\exp(-\gamma \frac{\Delta V}{heff})}$$

$$heff = \frac{V_F}{(V_{max}/h)_{intrinsic}}$$

$t(F)$: time to failure at application voltage
E_F: field at failure during ramp test
E_A: field due to applied voltage
V_F: voltage at failure during ramp test
V_F: voltage in application
Δt: ramp time step
ΔE: ramp field step
ΔV : ramp voltage step
$heff$: effective dielectric thickness
h: nominal dielectric thickness
$Vmax$: maximum V_F for nominal thickness
γ: acceleration factor

Fig. 3. The effective thickness model.

2. Root cause analysis

The initial root cause investigation was deliberately broad, due to the uncertainty in the timing of failures, and included areas such as the fabrication of the capacitors, mask errors, possible antenna effects, environmental conditions, and ESD. Standard failure analysis techniques such as optical and SEM inspections, FIB cross sectioning, and IR imaging were employed, as well as modeling of electric fields within the particular capacitor design and RF modeling of antenna effects.

Root cause failure analysis of shorted capacitors highlighted certain shared features which could be observed optically and microscopically. Optical features included discoloration at the wafer surface in the region around the capacitor. Microscopic features (from focused ion beam cross sections and STEM analysis) included etched or pitted capacitor dielectric and chemical extrusion from the surrounding area. Examples of these features are shown in Fig. 5.

Ramped voltage testing of PCM capacitors indicated that they had nominal reliability. These tests were performed on capacitors of varying size, and included both cap-over-via and no-via layouts. This data is plotted in Fig. 6. The fact that the PCM capacitors had much better reliability than those in the MMICs suggested that the specifics of the capacitor layout could contribute to the likelihood of failure.

3. Layer-by-layer analysis

The fact, noted above, that the PCM capacitors had nominal reliability indicated that the root cause was unlikely to be found in the nominal capacitor process of bottom plate, dielectric, and top plate depositions, and might be discovered by looking at the particulars of the failed capacitors.

Layer-by-layer analysis of the CAD layout of circuits containing shorted capacitors was performed in parallel with scrutiny of the HBT MMIC process. This analysis uncovered design features common to the majority of failed capacitors. In addition, it was noted that all capacitors could be grouped into categories defined by the details of their metal connections. Those three categories/connection types can be summarized as follows:

Type 1 — The capacitor is connected through on-wafer metal routing layers. No failures were observed on capacitors with this connection type (Fig. 7).

Type 2 — The capacitor is connected through metal-on-BCB routing. The connection is made through a BCB window directly to the top plate of the capacitor. A small percentage of failures were observed on these capacitors (Fig. 8).

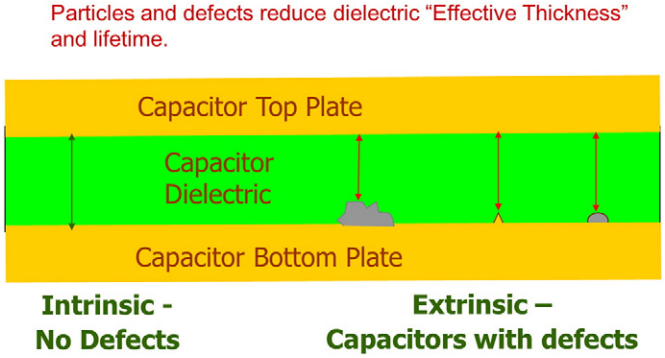

Fig. 2. A schematic of intrinsic and extrinsic capacitors.

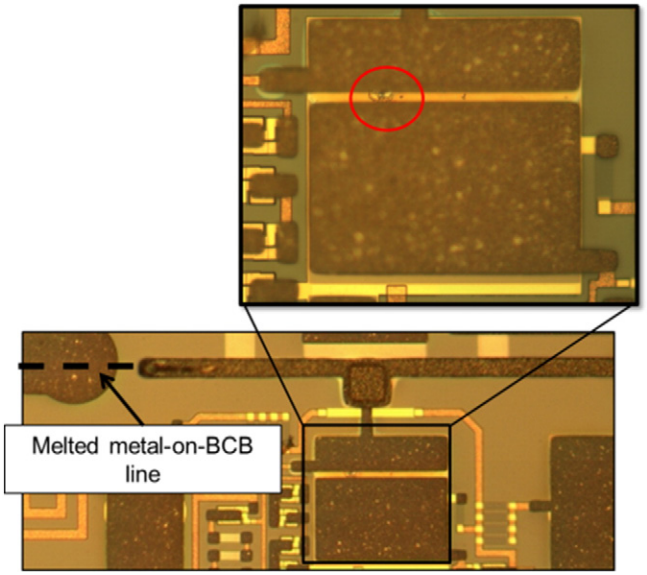

Fig. 4. Representative example of the failure signature common to the cap failures.