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Introductory Invited Paper

Equivalent circuit modeling of the bistable conduction characteristics in electroformed thin dielectric films

J. Blasco [a], N. Ghenzi [b], J. Suñé [a], P. Levy [b], E. Miranda [a,*]

[a] Departament d'Enginyeria Electrònica, Universitat Autònoma de Barcelona, Cerdanyola del Valles, Spain
[b] Departamento de Materia Condensada, GIA, GAIANN, CAC, Comisión Nacional de Energía Atómica, Buenos Aires, Argentina

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ABSTRACT

In the last few years a number of models based on simple circuital representations have been proposed to account for the resistive switching (RS) current–voltage (*I–V*) characteristics of metal–insulator–metal (MIM) structures. These devices typically exhibit two well-defined conduction levels after electroforming often referred to as the low and high resistance states that can be cyclically reached by the application of bipolar periodic voltage or current. The resulting hysteretic behavior arises from a reversible change of the electron transmission properties of the insulating film driven by an external stimulus. In this paper, after an overview of a variety of RS model proposals relying on circuital descriptions and basic analytic expressions, a model based on the solution of the generalized diode equation is discussed. The model is simple and flexible and consists of two opposite-biased diodes with series and shunt resistances that represent the filamentary current pathway spanning the oxide layer as well as the possible parasitic effects. The model parameters are governed by a mathematical entity called the logistic *hysteron* that can be linked to the internal state equation of the so-called memristive systems. For illustrative purposes, the switching *I–V* characteristics of TiO_2-based MIM structures electroformed with different current compliances are examined in detail using this approach. Experimental results on bipolar RS by other authors are also assessed within the same framework.

1. Introduction

The use of electroformed metal–insulator–metal (MIM) structures as the core elements in nonvolatile memories is currently considered a viable alternative for the implementation of high capacity information storage systems and logic applications [1–6]. This promising technology, called RRAM for Resistance change Random Access Memory, can adopt the form of stackable crossbar arrays and is the subject of extensive investigation by academia and industry worldwide [7–9]. The operational principle of these devices as memory elements relies on their ability to withstand the reversible formation and rupture of a single or multiple filamentary defect or metal paths spanning the dielectric layer for a large number of read-write cycles (>10^{10} [10]). The physical phenomenon is known as the resistive switching (RS) effect and has been observed in many binary transition metal oxides (TMO) and multinary oxides such as NiO [11–20], TiO_2 [21–36], HfO_2 [37–49], Ta_2O_5 [9,10,50–55], ZnO [56–61], SiO_x [62–65], CeO_x [66–68], Al_2O_3 [69], SnO_2 [70], ZrO_2 [71], MgO [72], Nb_2O_5 [73], Yb_2O_3 [74], $SrTiO_3$ [75–81], $Pr_{1-x}Ca_xMnO_3$ [82–84], and $La_{1-x}Ca_xMnO_3$ [85,86], among others. The simplicity, low cost, high endurance, fast switching time, scalability, multi-bit storage capability, controllable programming current and in some cases compatibility with conventional CMOS technology make RRAM devices serious contenders to memories based on charge transfer mechanisms such as flash [3,79,81,87]. However, in spite of these auspicious news, variability and reliability are still major concerns for oxide-based RRAMs [88–91].

One of the most accepted pictures for RS attributes the alternate formation and dissolution of the filamentary pathways to an electrochemical reduction–oxidation (REDOX) process occurring within the insulating matrix driven by an external electrical stimuli [2]. Modifications of the oxide layer at the interfaces with the electrodes caused by the accumulation of mobile charge may also be involved [58,77]. Memories based on this principle are referred to as Valence Change Memories (VCM). As the result of this electron-ion interplay, the oxide becomes more or less permeable to the electron flow with the consequent resistance change between a low (LRS) and a high (HRS) resistance state. A similar phenomenology has also been reported in the case of the formation and rupture of metallic-like filamentary paths [92,93]. This is the

* Corresponding author.

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operational principle of Conducting Bridge RAMs (CBRAM), also called Electrochemical Metallization Memories (ECM) or Programmable Metallization Cells (PCM), which are based on the relocation of metal ions within a solid electrolyte. The transitions HRS ↔ LRS can be abrupt (digital RS) or gradual (analog RS) indicating the sudden or progressive opening/closing of multiple parallel leakage paths or the narrowing/widening of the cross-section area of a single filament [4,94–97]. This latest property (tunable resistance) has been suggested for multi-level or multi-bit storage systems [54,71,98,99]. In general, the switching occurs after reaching certain threshold voltages with the same (unipolar RS) or with opposite (bipolar RS) polarities and they are called the SET (HRS → LRS) and RESET (LRS → HRS) voltages (see Fig. 1). The particular features of the switching processes seem to be related not only to the properties of the dielectric material but also to the metal electrodes and forming conditions. In addition, current compliances (CC) are often applied during the SET process in order to limit the thermal effects caused by the current runaway [26,100,101]. On the other hand, Joule heating at the bottleneck of the filament has been implicated in the dissolution mechanism of the conducting bridges, mainly for unipolar RS [51]. The first oxide breakdown event upon the application of electrical stress is called electroforming and corresponds to the generation of a localized weak oxide region susceptible to subsequent microscopic changes. From the statistical viewpoint, the electroforming event is fully consistent with the percolation theory of dielectric breakdown [90]. After this, the application of increasing and decreasing voltage sweeps leads to a pinched hysteretic behavior of the current–voltage (*I*–*V*) characteristic which has been often interpreted in terms of the memristor theory. This theory, which links electric charge and magnetic flux linkage in a device, was originally proposed by Chua [102], later reformulated for memristive systems by Chua and Kang [103], and finally extended by Chua himself to RRAM devices in 2011 [104]. Briefly, memristive systems are two-terminal circuit elements characterized by two coupled equations: one for the *I*–*V* curve of the device and one for its internal state variable [105–107]. While in linear systems the first relationship expresses an Ohmic-type dependence, the second one is written as a time derivative in order to account for the previous history of the device. The *I*–*V* model can be extended to nonlinear devices satisfying $I(V=0)=0$ and the state variable can be multidimensional [108]. Importantly, the connection between memristors and RRAMs has not been exempt from criticism and is still matter of debate [109,110]. In addition, it has been widely recognized the correspondence of the HRS and LRS with the soft-breakdown (SBD) and hard-breakdown (HBD) conduction modes occurring in thin dielectric films [64,86]. Both the SBD and HBD modes have been thoroughly investigated in ultrathin ($t_{ox} < 5$ nm) SiO_2 layers as well as in thicker high permittivity (high-κ) dielectrics used as gate insulators in MOSFET devices [111]. Physical models for the filamentary conduction in SiO_2 and high-κ films have been reviewed in Ref. [112].

However, in spite of the major technological advances and better understanding of the physics behind RS achieved during the last few years, simple and flexible analytic models able to account for the wide variety of switching *I*–*V* curves exhibited by different dielectric films and electrode materials are hard to find in literature. While some of the available approaches are difficult to implement in circuit simulators because of the complexity of the physical processes involved or the mathematical constraints in the model equations and its derivatives [15,107,113–117], other models only focus the attention on the HRS and LRS *I*–*V*s separately, completely disregarding the gradual transition between both states that in many cases characterizes the RS phenomenon. Other approaches are exclusively aimed at describing the SET and RESET switching dynamics caused by the application of current or voltage pulses [118–120]. Many SPICE-oriented models for RS have been recently reported [93,106,107,121–125], but their ability to accurately represent not only the electron transport characteristics in different materials but also their specific memory properties when subjected to arbitrary input signals has been seriously questioned [126]. Since the publication of Strukov's memristor model in 2008 [127], a number of simple approaches based on combinations of linear, nonlinear and rectifying devices have been developed to describe the bistable conduction characteristics of electroformed MIM devices. Some of them are reviewed in Section 2. In Section 3, a simple circuital model for the hysteretic *I*–*V* characteristics is extensively discussed. The proposed approach consists of two opposite-biased diodes with series and shunt resistances that represent the filamentary current pathway spanning the oxide layer and the possible parasitic effects. Earlier versions of this model were reported elsewhere [128,129]. It is worth pointing out that, in this work, the emphasis is on the representation of the *I*–*V* curves rather than on the physics foundations of the RS electron transport mechanisms. The objective is to achieve a flexible, continuous and derivable model expressible by means of analytic functions. In order to reproduce the hysteretic behavior caused by the application of bipolar periodic voltage, the diode parameters in our model are driven by a mathematical entity referred to as the logistic *hysteron* (see Fig. 2a). As it is shown in Section 3, this entity, in its simplest form, can be written as a state equation for memristive systems. The *hysteron* concept within the present context comes from the celebrated Preisach model for the hysteretic *B*–*H* curve of ferromagnetic materials [130]. The relay *hysteron*, which is the fundamental building block of the Preisach model, describes the instantaneous activation and deactivation of a memory element with threshold voltages α and β (see Fig. 2b). Here, the suitability of a smoothed version of this mathematical tool is demonstrated. The extension of the proposed

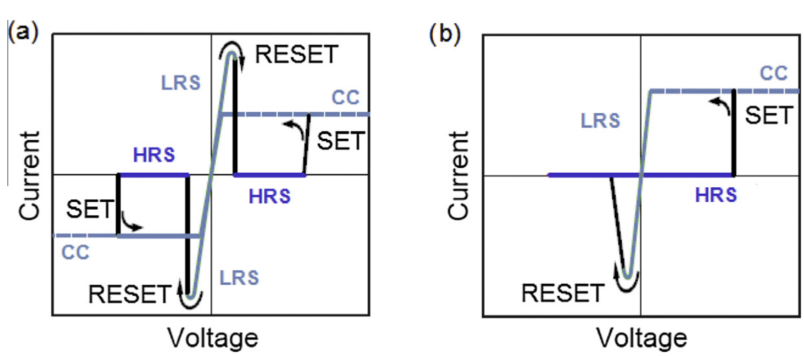

Fig. 1. The two basic resistive switching schemes: (a) unipolar RS and (b) bipolar RS. CC is the current compliance limit. HRS and LRS correspond to the high and low resistance states, respectively.