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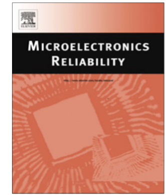

Introductory Invited Paper

Soft errors in floating gate memory cells: A review

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ABSTRACT

Soft errors due to neutrons and alpha particles are among the main threats for the reliability of digital circuits operating at terrestrial level. These kinds of errors are typically associated with SRAMs and latches or DRAMs, and less frequently with non-volatile memories. In this paper we review the studies on the response of NAND and NOR Flash memories to ionizing particles, focusing on both single-level and multi-level cell architectures, manufactured in technologies down to a feature size of 25 nm. We discuss experimental error rates obtained with accelerated tests and identify the relative importance of neutron and alpha contributions. Technology scaling trends are finally discussed and modelled.

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1. Introduction

Our society relies heavily on the correctness of digital computations, especially for safety-critical operations. A soft error, i.e. the corruption of a memory element due to scattered ionizing particles, can possibly lead to life-threatening situations and/or to large economic losses. In terrestrial applications, neutrons originating from the interactions of cosmic rays with the outer layers of the atmosphere and alpha particles emitted by radioactive materials in the chip and package materials are the main sources of soft errors [1].

Historically, the first observation of soft errors has been made on Dynamic Random Access Memories (DRAMs) [2]. More recently, Static Random Access Memories (SRAMs) and latches have received most of the attention [1], whereas non-volatile memories are (were) generally believed to be immune from soft errors.

The market of non-volatile memories is dominated by Flash devices. These components use Floating Gate (FG) transistors integrated in large arrays, with either a NOR or NAND architecture. NOR are mainly used for code storage, where random access is of primary importance. On the other hand, NAND Flash memories are suitable for applications where large amounts of sequential data need to be stored in a non-volatile way.

To increase the density, Multi-Level Cell (MLC) devices have been introduced to store multiple bits per cell, alongside Single Level Cell (SLC) memories. MLC devices have generally lower retention and endurance specifications, because of the smaller error margins. Nevertheless, MLC components are very attractive due to their large capacity and reduced cost per bit.

Reliability issues (such as program disturb, read disturb, quantum-level noise and stress induced leakage current) are becoming increasingly important as technology scaling leads to cells with smaller amounts of stored charge [3]. In parallel, concern about sensitivity to soft errors has been growing also in these devices, in addition to SRAMs, as the number of carriers in the FG reaches few tens.

Studies on radiation effects in Flash devices have begun in the 80s [4,5] and continue to this date, but the first evidence of atmospheric neutron-induced soft errors in MLC Flash NAND memories was reported only in 2008 [6]. Afterwards, a few publications have addressed the effects of the terrestrial neutron environment on both NAND and NOR [7–10] showing a consistent trend towards increasing neutron cross sections as the cell dimensions scale down. More recently, MLC NAND Flash memories with feature size equal to or smaller than 50 nm have been shown to be sensitive to alpha particles [10,11].

The purpose of this paper is to review the published data on neutron and alpha particle sensitivity for state-of-the-art Flash memories with feature size down to 25 nm. We will present the dependence of the error rate on the program level, compare the cross sections of MLC and SLC devices, and calculate the expected error rates in the terrestrial environment and at aircraft altitudes, with different amounts of contaminants. Finally, scaling trends will be investigated and predictions for sensitivity to soft errors of future-generation memories will be discussed.

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2. Neutron-induced FG errors

Fig. 1 shows a compilation of raw bit error cross sections (σ) as a function of the feature size published in the last few years [6,8,10]. The data reported in the plot have been obtained by exposing Flash memories produced by major vendors to atmospheric-like neutrons, at wafer or package level. The feature size of the tested devices ranges from 90 nm down to 25 nm. All the data were collected without using Error Correction Codes (ECC), which are required for NAND devices, due to the non-zero bit error rate [3], as will be discussed later. Most of the data were obtained with wide-energy spectrum neutrons at the VESUVIO line of the ISIS accelerator at the Rutherford Appleton Laboratories, in Didcot, UK. In this facility, neutrons are obtained by spallation reactions from 800-MeV protons colliding with a tungsten target. The VESUVIO neutron spectrum partially reproduces the terrestrial neutron environment, with several orders of magnitude of acceleration.

Memories were programmed and read prior to neutron exposure (errors even without radiation were present in some devices), irradiated unbiased at room temperature, and then read again. Through unbiased irradiation, errors in FG cells can be studied, as no single event effects happen in the control circuitry. Post radiation measurements were performed generally within few weeks after exposure. The MLC FG cells were programmed with logic checkerboard patterns, using all the four program levels. Fig. 1 presents the average error cross sections. For SLC samples, the cells were generally set to the programmed state ('0') before irradiation and so the cross section refers to that level.

As seen in Fig. 1, the bit error σ increases with an exponential trend, as the feature size is reduced. From 90-nm to 25-nm, the error rate increases by almost four orders of magnitude in MLC Flash. SLC memories are much less sensitive. Errors were reported already at the 65-nm node, but σ was almost negligible, and only at a feature size of 34 nm the cross section becomes significant. It is interesting to compare the cross sections of Flash, as far as soft errors are concerned, with those of the benchmark component, SRAM. The σ of SRAMs is typically around 10^{-14} cm^2, a value that is similar to that of the 25-nm MLC Flash.

Neutron life tests experiments were also performed on Flash memories. Fig. 2 shows the results of a 18-month experiment on NOR devices [9]. The difference between the cells kept underground, shielded from atmospheric neutrons, and those stored at an altitude of 2552 m, where the neutron flux is higher than at sea level, is evident, even though the number of errors is too small to draw quantitative conclusions.

Concerning the dependence of the errors on the program level, generally the higher the program level, the higher the sensitivity. A significant deviation from this behavior was found in some recent 25-nm devices [11]. In fact, for these 25-nm samples the neutron sensitivity is roughly the same for all program levels, whereas for 65-nm and 90-nm MLC NAND, the highest level is considerably more sensitive than the lower threshold voltage (V_{th}) levels. This is depicted in Fig. 3 [10], where the levels are indicated with L0 (erased), L1, L2, and L3, from the lowest to the highest V_{th}.

Possible differences in the neutron cross sections when the samples are irradiated from the front-side or from the back-side were also investigated in [10]. Variations in the front- and back-irradiation bit σ is always below 20% and negligible for many samples.

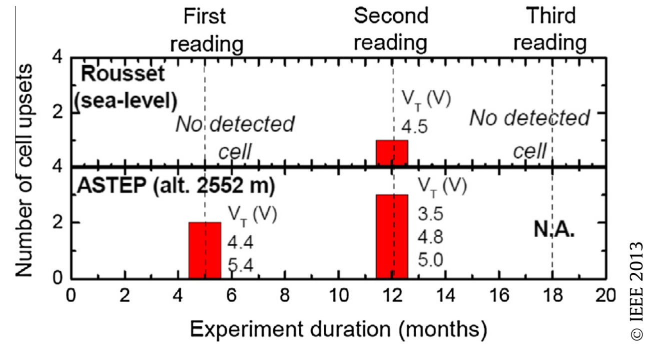

Fig. 2. Number of memory cells with shifted threshold voltage below the reference value (5.7 V) delimiting the "0" and "1" logical states, for NOR Flash devices irradiated with neutrons. After [9].

3. Alpha-induced FG errors

In addition to neutrons, also alpha particles can lead to soft errors in electronic chips in the terrestrial environment. These particles are emitted by radioactive contaminants that are inevitably present in the chip and package materials. Some Flash devices have been shown to be sensitive also to alpha particles. In [11], NAND memories were exposed to alphas emitted by a radioactive 241-Am source. The energy of the alpha particles at the chip surface was about 5.4 MeV, (corresponding to a Linear Energy Transfer, LET, of 0.7 MeV cm^2/mg). All irradiations were performed at room temperature on unbiased samples with shorted pins.

Fig. 4 illustrates the raw bit error cross section, for MLC and SLC devices [11]. Similar to the neutron case, MLC samples were irradiated with FG cells distributed in all four V_{th} levels and the cross sections in Fig. 4 are averaged over all the levels. As seen, for MLC samples, the alpha-induced error cross section is about 3 orders of magnitude larger with respect to the neutron one. From

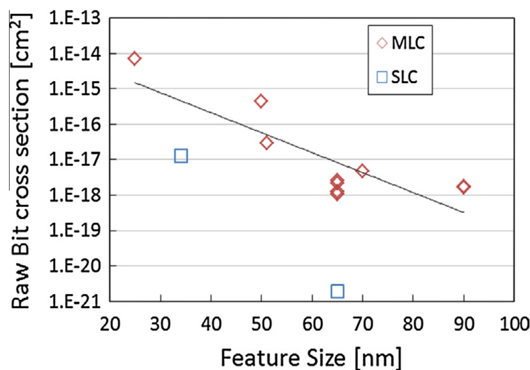

Fig. 1. Compilation of cross section data for MLC and SLC NAND Flash. Results are taken from [6,8,10].

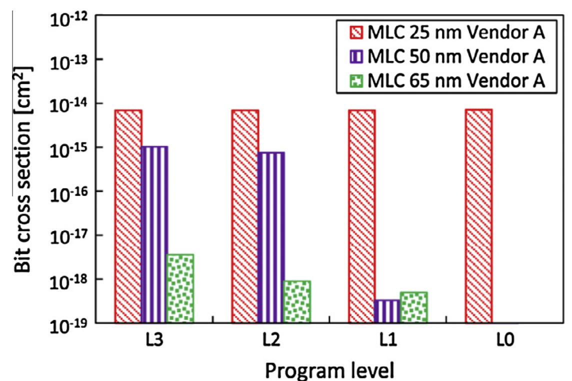

Fig. 3. Cross section for neutron-induced errors as a function of program level (L0, L1, L2, L3, from the lowest to the highest threshold voltage) in MLC NAND Flash samples. After [10].

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