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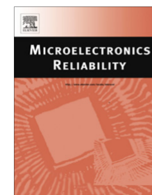

Reliability impacts of high-speed 3-bit/cell Schottky barrier nanowire charge-trapping memories

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ABSTRACT

This study experimentally examines the reliability impacts of high-speed 3-bit/cell Schottky barrier nanowire charge-trapping memories. Unique Schottky barrier junctions strongly enhance hot-carrier generation, ensuring high-speed multi-level programming at low gate voltages. However, strong injected gate currents might cause potential retention and endurance concerns when the programming voltage is beyond 9 V. The effective number of deep-level traps is insufficient for capturing injected electrons, such that some electrons occupy shallower states, producing retention degradation after thermal stress. The charge-trapping layers are susceptible to additional trap generation under strong gate currents, leading to considerable threshold-voltage shifts after cycling stress. A compromise of cell characteristics exists between excellent reliability and high-speed programming in 3-bit/cell Schottky barrier nanowire cells. The application of sub-8-V multi-level programming can alleviate the potential reliability generated by strong injected currents, preserving a favorable cycling endurance and thermal retention in 3-bit/cell Schottky barrier nanowire charge-trapping cells.

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1. Introduction

Nanowire devices have gained increasing attention from the semiconductor industry for outplacing planar and FinFET devices in future CMOS technologies because of their ultimate gate control against the short-channel effect [1–3]. For use in 3D memories to increase the packing density, advanced nonvolatile Flash technology has migrated from planar float-gate cells to nanowire charge-trapping silicon–oxide–nitride–oxide–silicon (SONOS) structures [4–12]. However, the advancement of charge-trapping cells remains limited by the need for high-voltage programming or erasing through Fowler–Nordheim tunneling. The conventional SONOS cell is also unsuitable for use in NAND-Flash memory because of its relatively high hole tunnel-barrier [12,13,9]. A compromise of cell characteristics exists between poor retention and slow erasing in traditional SONOS cells.

Even if an operation voltage of up to 20 V might be feasible in NAND-Flash technologies, aggressive voltage scaling is desirable in practical 3D memories, particularly in multi-bit-cell applications. With breakthroughs in low-voltage operations, a previous study on innovative programming and erasing proposed pure Schottky barrier nanowire SONOS cells to demonstrate aggressive scaling in operation voltages [14,15]. The unique Schottky barrier junctions enhance hot-carrier generation substantially, thereby ensuring low-voltage programming and erasing [16–18]. By using a particular ambipolar conduction of Schottky barrier devices, the Schottky barrier SONOS cells can operate at gate voltages of 5–7 V for electron programming, and −7 to −9 V for hole erasing through Fowler–Nordheim-mode tunneling [14,15,19,20].

For Schottky barrier SONOS cells, the physical mechanisms of cell operations are relatively intricate because the electron and hole carriers are involved in cell programming and erasing, and their tunneling always locates the same spots at the source- and drain-side edges of the channel. Strong injected currents and unique operations might generate specific reliability concerns regarding Schottky barrier cells on the thermal retention and cycling endurance. When the multi-bit-cell application is employed to increase the bit/cell density of Schottky barrier SONOS cells, the operational voltages must be raised to increase injected gate currents, ensuring sufficient threshold-voltage shifts at a favorable speed. The tradeoffs inherent in speed performance and cell reliability necessitate optimizing operation voltages in multi-bit/cell Schottky barrier SONOS cells, and the favorable speed and adequate reliability must be considered concurrently.

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This paper first examines the reliability impacts of high-speed 3-bit/cell Schottky barrier SONOS cells, and subsequently presents an alternative approach to resolve the reliability concerns by using reliable low-voltage programming. The tradeoffs between the programming speed and cell reliability are then elucidated. Section 2 details the process fabrication and device parameters used in experimental studies. The cell operations required to perform the programming and erasing of 3-bit/cell Schottky barrier SONOS cells are discussed. Section 3 presents the measured results of high-speed 3-bit/cell nanowire SONOS cells, with an examination of the potential degradation mechanisms of cell reliability. Section 4 presents the experimental results of reliable 3-bit/cell Schottky barrier nanowire SONOS cells under low-voltage programming, and offers a discussion on the tradeoffs between the programming speed and cell reliability in multi-level Schottky barrier nanowire SONOS cells.

2. Cell structure and operation

2.1. Cell structure and process fabrication

Fig. 1(a) depicts the schematic structures of Schottky barrier nanowire SONOS cells. Gate-all-around nanowire was adopted with a poly-Si gate and channel. A hard-mask sidewall oxide spacer was employed to fabricate the gate-all-around nanowire structure without necessitating advanced lithography. Detailed steps and schematics for fabricating the Schottky barrier nanowire SONOS devices can be found in [14,15]. After an amorphous silicon layer was deposited and transformed through solid-phase crystallization into a Poly-Si layer, a sacrificial TEOS oxide was formed and patterned. Followed by hard-mask nitride deposition, the metallic source/drain region was defined to expose the non-silicidation nanowire. The nitride spacer was formed to define the underlying silicon nanowire. Recessed oxide etching was then performed to produce the gate-all-around nanowire channel. After the oxide/nitride/oxide (ONO) layers and n + Poly-Si gate were fabricated, the gate spacer and nickel silicidation were conducted to form the NiSi Schottky barrier source/drain.

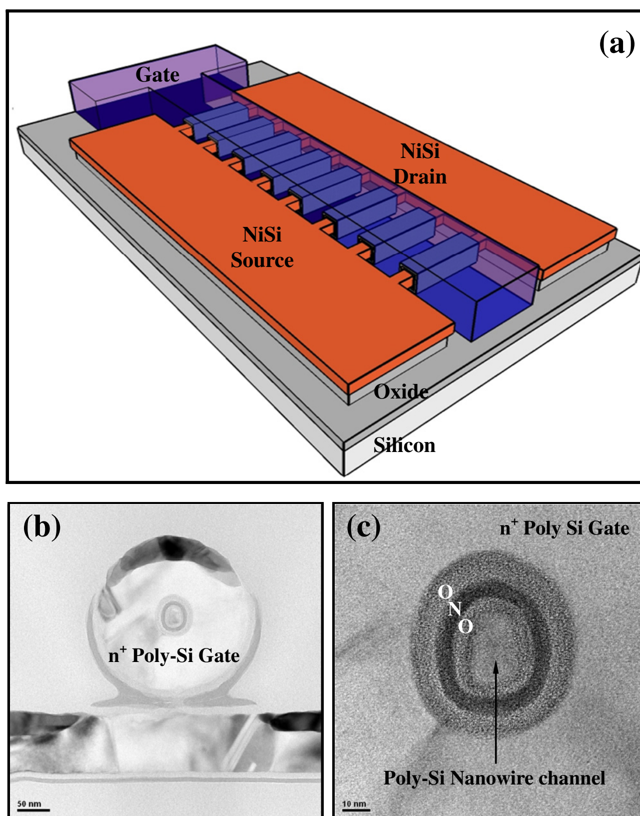

Fig. 1. (a) Schematic structures of Schottky barrier nanowire SONOS cells. (b) Cross-sectional TEM image of a fabricated Schottky barrier nanowire SONOS cell. (c) Enlarged TEM image of nanowire channel and ONO layers.

Fig. 1(b) presents the cross-sectional transmission electron microscopy (TEM) image of a fabricated Schottky barrier nanowire SONOS cell. As-grown ONO layers of 4 nm, 6 nm, and 10 nm were deposited as charge-chapping layers. Fig. 1(c) shows an enlarged TEM image of the nanowire channel and ONO layers. Conventional nickel silicidation was conducted to form the metallic source/drain [21]. Thermal oxidation was performed at 900 °C to grow the tunneling oxide. Low-pressure chemical vapor deposition (LPCVD) was employed at 780 °C and 700 °C to form nitride and blocking oxide layers, respectively. Eight-wire nanowire cells with a length of 1 μm were measured to examine the programming, erasing, and reliability characteristics.

2.2. Electron programming and hole erasing

Fig. 2 shows the measured current–voltage curves of the fabricated Schottky barrier nanowire SONOS cells. Conduction can be enabled in both electron and hole channels in Schottky barrier nanowire cells by using appropriate gate voltages. At positive gate voltages, the electron carriers tunnel through the source-side Schottky barrier, and travel along the nanowire channel. At negative gate biases, the holes can pass through the drain-side Schottky barrier, yielding a hole drain current.

Both electron and hole currents can be sufficiently high to generate strong hot carriers for injections. At sufficiently positive gate voltages, the Schottky barriers, formed at the source and drain edges, can induce abrupt conduction-band bending and an associated large lateral electrical field to produce a substanti amount of hot electrons for programming. To erase the Schottky barrier cells on both edge sides, the cell is then switched to operate at a negative gate bias. The Schottky source/drain barriers induce a substantial lateral electrical field around the source-/drain-side region to generate considerable hot holes for erasing. Because of the substantial promotion of hot electrons and hot holes generated by the lateral Schottky source/drain barriers, strong gate currents are injected at the source-side and drain-side edges for efficient programming and erasing. Because the hot electrons and hot holes are created only at the source and drain edges, the charge storages

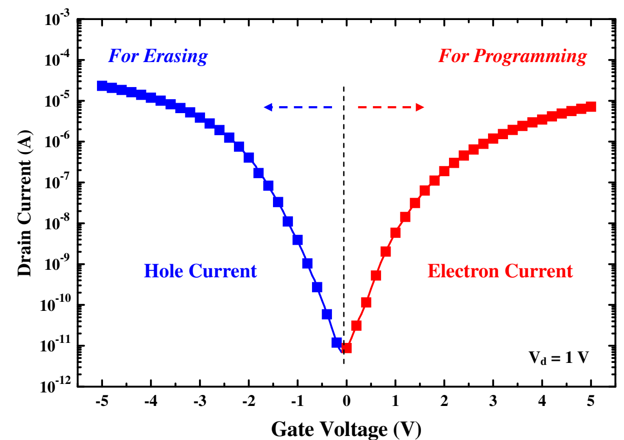

Fig. 2. Ambipolar current–voltage curves in fabricated Schottky barrier nanowire SONOS cells.

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