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Characterizing, modeling, and analyzing soft error propagation in asynchronous and synchronous digital circuits

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ABSTRACT

Soft errors, due to cosmic radiations, are one of the major challenges for reliable VLSI designs. In this paper, we present a symbolic framework to model soft errors in both synchronous and asynchronous designs. The proposed methodology utilizes Multiway Decision Graphs (MDGs) and glitch-propagation sets (GP sets) to obtain soft error rate (SER) estimation at gate level. This work helps mitigate design for testability (DFT) issues in relation to identifying the controllable and the observable circuit nodes, when the circuit is subject to soft errors. Also, this methodology allows designers to apply radiation tolerance techniques on reduced sets of internal nodes. To demonstrate the effectiveness of our technique, several ISCAS89 sequential and combinational benchmark circuits, and multiple asynchronous handshake circuits have been analyzed. Results indicate that the proposed technique is on average 4.29 times faster than the best contemporary state-of-the-art techniques. The proposed technique is capable to exhaustively identify soft error glitch propagation paths, which are then used to estimate the SER. To the best of our knowledge, this is the first time that a decision diagram based soft error identification approach is proposed for asynchronous circuits.

1. Introduction

With the scaling of process technologies, the ratio between the charge required to introduce a current pulse that changes a logic state, i.e. the critical charge (Q_{CRIT}), and the charge collection efficiency (Q_S) has been reduced significantly [1,2]. Therefore, the possibility of transient pulse generation, when an energetic particle hits one of the sensitive sites of a combinational logic block or of an asynchronous circuit, has considerably increased in modern deep sub-micron (DSM) technologies. This phenomenon is known as a single event transient (SET). These transients may cause reversible (soft) and irreversible (hard) faults in digital designs, which are often called Single Event Effects (SEEs). Soft faults are more difficult to trace because it is hard to reproduce. If a soft fault results in changing the state of a system, then it leads to soft errors. Hence, with technology evolution, the soft error rate (SER) has become an important reliability metric and there is a growing need for fast, accurate, and efficient estimation of that metric.

Soft faults and the resulting soft errors are traditionally studied at the physical design level. On the other hand, it is desirable to develop a technique for SER estimation at a higher abstraction level. Recently, some groups have developed methodologies to perform SER estimation at the gate level or higher. One of those techniques is to do simulations with fault injection based on random vector generation [3–5]. However, the simulation based approach has serious shortcomings as fault simulations can be very time consuming for large designs with many primary inputs and sequential states. When complexity forces using sampling techniques, accuracy of fault simulations decreases with the ratio of the simulated sample size over the total vector space size.

Another technique used for soft error modeling and estimation is based on binary decision diagrams (BDDs) [6–8]. BDDs notoriously suffer from a state space explosion problem. In [9], the authors proposed the combinations of the reduced-order binary decision diagrams (ROBDDs) and the algebraic decision diagrams (ADDs), to simultaneously model and analyze the effects of logical, electrical, and time masking. However, the use of two decision diagrams makes this technique more complex and it consumes a considerable amount of memory. Recently, a new technique was proposed in [10], which leverages the concepts of Boolean Satisfiability and uses the so-called SAT (satisfiability) solvers. In

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spite of the use of very efficient SAT solvers, this method is time consuming and resource hungry, partly because of the requirement of unrolling copies of the circuit when modeling sequential designs.

Notably, none of the above mentioned approaches deal with asynchronous handshaking circuits, which have recently become a popular solution for clock domain crossing (CDC) interfaces. The utilization of asynchronous handshakes will increase once emerging arbitration schemes are fully evolved [1]. Moreover, 25% of the global signals in integrated circuits will use asynchronous handshakes [28]. Since asynchronous interfaces use combinational logic and feedback, they are more vulnerable than combinational logic to soft error glitches that may result from poor signal integrity. In certain cases, errors occurring in asynchronous circuits can have catastrophic effects due to the event ordering constraints that may cause circuit failures or deadlocks [11]. Therefore, analyzing the sensitivity to soft errors in asynchronous circuits early in the design cycle is a growing concern. As a step in that direction, in [30], a new simulation based methodology to analyze the Quasi-Delay Insensitive (QDI) asynchronous circuits is proposed. In that method, probability distributions and confidence intervals are used to decrease the total number of simulations.

In order to overcome these shortcomings, a new methodology to characterize, model, and analyze soft error propagation at gate level is proposed. This work is distinct in the following ways:

(1) A new technique is proposed to model soft error glitch propagation in digital designs using Multiway Decision Graphs (MDGs) [12]. MDGs are chosen over other types of decision graphs because they allow defining several data types, which are used to capture different characteristics related to glitches. The enumerated data type in MDG facilitates modeling both the notion of soft error glitch width variation e.g., electrical masking and the sensitization path e.g., logical masking in a single decision diagram.
(2) It is demonstrated that the proposed technique models the expected circuit behavior in case of soft error glitches utilizing only gate level information. This methodical approach is fully automated in new tool called SEGP-Finder. This technique can be used by designers to facilitate insertion of error-mitigation mechanisms on selected control and data paths. Moreover, this work identifies the set of conditions that may lead to soft error propagation; hence it reduces the requirement of having controllable or observable nodes, which may be necessary from a design for testability (DFT) perspective. Consequently, considering these conditions may reduce the need for complete and more expensive redundancy techniques, such as systematic triple module redundancy (TMR).
(3) In this methodology, we combine the adopted SER estimation algorithm (similar to [10]) and our proposed soft error glitch propagation analysis. This combination leads to a more accurate analysis, where less memory is required than contemporary techniques (such as [10]). This improvement is mainly due to the use of the MDG model checker as a verification engine in our algorithm. The MDG tool is applicable to different kinds of systems, some of which as large as 11400 gates, as shown by different case studies [14–16].

The rest of this paper is organized as follows. Section 2 reviews the literature on the MDG decision graph, the MDG model checker, and asynchronous interfaces. Section 3 explains in details how the principle of GP set and MDG are extended to model both electrical and logical masking effects of soft errors. Section 4 explains the proposed methodology. In Section 5, applications of the proposed methodology on combinational logic, sequential logic, and asynchronous circuits are explained. Section 6 describes the proposed automated tool supporting this methodology. Section 7 provides results and a discussion. Finally, Section 8 concludes this paper.

2. Preliminaries

We choose MDG to model soft error glitch propagation paths in digital designs utilizing glitch propagation (GP) sets [13]. In this section, a background is provided about terminologies frequently used in this paper:

2.1. Multiway Decision Graphs (MDGs)

It is an extension of BDD in the sense that it represents and manipulates a subset of first-order logic formulae suitable for large data-path circuits. One of the advantages of MDG over other representations is that a data value can be represented by a single variable of an abstract type; whereas, BDD and ROBDD based methodologies such as MARS-C [9] and MARS-S [26] can only use concrete Boolean variables. The enumerated data type in MDG facilitates modeling both the logical and electrical masking of soft error glitches in a single decision diagram; MARS-C [9] and MARS-S [26] use separate BDDs for each masking effect. The data operation in MDG can be represented by a function symbol, which can apply to a pre-defined data type.

2.2. MDG Tool Set

It is a tool set for the formal verification of digital systems that is based on MDG. It has been used to verify a number of complex systems [14–16]. It includes application procedures for combinational and sequential equivalence checking [12], model checking [17], and invariant checking [12]. Our methodology utilizes the invariant checking tool, which is a formal verification approach that performs reachability analysis to check the potential of system failure due to a particular fault under specified conditions. If the fault exists, then an example is generated to demonstrate the condition under which the system may fail (such examples where a property fails are commonly called counterexamples of some property). Moreover, the invariant checking tool in the MDG tool set allows analyzing the propagation of an injected soft fault in one version of the design, without the need for two versions of the design (faulty and error-free versions) as required with the BDD based techniques [9,26].

2.3. Asynchronous Handshake Protocols

A digital system with asynchronous interfaces for interaction between (internally) synchronous modules is known as a globally asynchronous locally synchronous (GALS) system. Several asynchronous interfaces have been proposed for GALS. Broadly, based on their handshake protocols, these interfaces can be divided into two classes, the bundled data protocols [18,19], and delay-insensitive (DI) data-encoded protocols [20]. Bundled data protocols consist of separate request and acknowledgement signals that may utilize return-to-zero or non-return-to-zero signaling, assuming the data travels on a separate bus. DI data-encoded protocols combine the request and data signals; hence data does not have to abide any separate signal timing constraints. The acknowledgement signal, in DI handshake, is similar to many other asynchronous handshakes. Further details on some representative asynchronous handshake circuit implementations are provided in Section 5.2.