Microelectronics Reliability 53 (2013) 2070–2077

Contents lists available at SciVerse ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/microrel

Delay fault testing using partial multiple scan chains

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ARTICLE INFO

Article history:
Received 19 February 2013
Received in revised form 28 June 2013
Accepted 3 July 2013
Available online 1 August 2013

ABSTRACT

Delay test patterns can be generated at the functional level of the circuit using a software prototype model, when the primary inputs, the primary outputs and the state variables are available only. Functional delay test can be constructed for scan and non-scan sequential circuits. Functional delay test constructed using software prototype model can detect transition faults at the structural level quite well. Therefore, we propose a new iterative functional test generation approach. The proposed approach involves a partial multiple scan chain construction using the results of functional delay test generation at a high level of abstraction. The iterativeness of the method allows finding the compromise between the test coverage, hardware overhead and test length. Furthermore, using the partial multiple scan chains requires less hardware overhead resulting in shorter test application times. The experimental results are provided for the ITC'99 benchmark circuits. Experiments showed that the obtained transition fault coverage is on average 2% higher than using full scan and commercial automatic test pattern generator for transition faults.

1. Introduction

Testing of sequential circuits is a complex problem to solve but the testability of sequential circuits has been improved through the use of design for testability technique called scan chain insertion. The most prevalent scan insertion method is a full scan since it reduces the sequential circuit test generation problem into a combinational one. In the full scan, each flip-flop is modified into a scan flip-flop and connected into a scan chain that allows straightforward scan-in and scan-out of test patterns. However, the full scan incurs area overhead, reduced circuit performance, and considerable increase of test application time. Insertion of as many multiplexers as the number of flip-flops in the design obviously imposes a considerable area cost. Furthermore, these multiplexers are inserted on functional paths, resulting in critical path prolongation by a multiplexer delay, and hence it introduces extra delay to the circuit. Many clever scan flip-flop designs have been implemented over the years, which minimize this performance penalty, but there always are critical circuits that cannot tolerate any loss of the performance. When the full scan is used, every test pattern consists of as many bits as the number of flip-flops in the design. Moreover, every such test pattern has to be serially shifted in using extra scan-in input. The results are observed at the extra scan-out output. Therefore, the test application is increased very considerably.

When certain flip-flops are not replaced with scan flip-flops, the result is a partial-scan circuit. The partial-scan solves many problems of the full scan. Removing scan multiplexers corresponding to some of the flip-flops reduces the area cost, potentially improves the circuit performance, and reduces the scan path length, thus, decreasing the test application time and the test data volume. But partial-scan introduces specific problem. As a result, controllability and observability of the unscanned flip-flops are compromised, necessitating sequential automatic test pattern generation (ATPG). The computational cost of sequential ATPG cannot be afforded, keeping in mind the complexity of today's integrated circuits. Therefore, only computationally efficient partial-scan can replace the full scan [1].

We propose to construct the computationally efficient partial-scan at the functional level of the circuit. The functional level allows considering the circuit at the high level of abstraction. The circuit at the functional level is not related to the particular implementation. Additions to the circuit at the functional level concerning the testability then are integrated to the circuit during the synthesis. Hence, the timing, area, and performance are optimized for the circuit during the synthesis process. This means that the structure of the circuit is built for effective delay scan testing.

In this paper, we present a novel method to construct a partial multiple scan (PMS) chains using the results of the functional test generation. The information concerning the sensitivity of the flip-flops is collected during the functional test generation. This information is used to construct partial-scan chains for delay fault testing such that the overhead and test application time are minimized. The method enables sharing functional primary inputs

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http://dx.doi.org/10.1016/j.microrel.2013.07.002

with scan-in inputs and functional primary outputs with scan-out outputs. The method requires only single extra scan-enable input.

The rest of the paper is organized as follows. We review the related work in Section 2. We recall the functional fault model in Section 3. We propose a method for the construction of PMS chains in Section 4. We present the scheme of using software prototype models in the process of functional test generation in Section 5. We report the results of the experiment in Section 6. We finish with conclusions in Section 7.

2. Related work

For many years, the world-wide standard solution for structural digital test was use of the scan methodology. The scan-based technology is used to detect stuck-at faults and transition faults. Two test vectors are applied to detect transition faults, namely $v1$ and $v2$. The first vector $v1$ initializes the internal logic of circuit to a certain state, while the second vector $v2$ launches transitions at the targeted nodes in the next clock cycle, and the response of the circuit is then captured at-speed to verify the correctness of the timing requirements. The primary scan-based test techniques are enhanced scan (ES) [2], launch-on-shift (LOS) [3], and launch-on-capture (LOC) [4].

In the ES method, the scan flip-flops have the ability to store two individual test patterns whereas other architectures can only store one test pattern. The ES allows the scan and application of any two-pattern test without imposing any scan architecture constraints. Although high transition fault coverage can be attained with relatively small size set of test pattern by the ES method, it is rarely used in the modern VLSI chips for the unacceptable hardware overhead [5].

In the LOS scan architecture, test pattern $v2$ is simply test pattern v1 shifted by one bit. This requires the scan-enable to operate at the frequency of the chip. Unfortunately, due to the requirement of timing critical scan-enable signal, this approach is not adopted by most scan-based designs [6].

LOC overcomes the limitations of ES and LOS, and has been widely adopted in industrial applications. Under the LOC scan architecture, the second pattern $v2$ is a functional response to the first pattern $v1$. The scan-enable signal is activated and the first pattern is scanned in. The first pattern is then applied and the response is captured by scan cells, producing pattern $v2$ (launch pattern). Although LOC method has low implementation cost, the transition fault coverage can hardly achieve a satisfactory level due to the architectural restriction for generating the launch vector $v2$. Moreover, large numbers of inputs may need to be specified in the initialization vector for setting the specific state input to a required logic value in the launch time frame due to the function dependency. Therefore, the volume of generated test patterns is typically very large in the standard LOC delay testing approach.

Based on respective advantages of the above mentioned three delay testing methods, several techniques have been proposed by combining these methods to improve transition fault coverage and reduce the number of transition delay test patterns with relatively low hardware overhead. The suggested approaches can be broadly classified into two categories: hybrids of LOS and LOC mechanisms, and partial enhanced scan. Wang et al. [7] presented a hybrid delay scan scheme, in which a small number of flip-flops are selected to be controlled by the LOS approach using a flip-flop selection algorithm. The rest scan cells are then operated in the LOC mode. Xu and Singh [6], Ahmed et al. [8] suggested to insert a new logic into scan chains to align the slow scan-enable signal to the clock edge. Park et al. [9] proposed a scan delay scheme, in which the launch-on-shift-capture (launch-on-capture-shift) test is a three-pattern test for transition faults that launches transitions by both launch-on-shift and launch-on-capture mechanisms. The method [9] is more complicated since it requires propagating fault effects over two time frames rather than one time frame of the conventional LOS test.

The methods of the second category employ enhanced scan, but partial. They vary mainly by the selection strategy which cells of the scan have to be enhanced. Devtaprasanna et al. [10] proposed to select a subset of flip-flops to be replaced with enhanced scan cells based on the fault sets which can be detected by enhanced scan approach but not by standard LOC approach. Xu et al. [11] suggested using the controllability measure in order to replace a limited number of regular scan cells with enhanced scan cells. Wang et al. [12] suggested using the controllability and usefulness measures. The approach of measures is used in [13], as well. Pei et al. [13] calculate the 0 (1) relative measure of a regular scan cell, which consists of the 0 (1) activation relative measure and 0 (1) propagation relative measure representing the number of testable transition faults under fault collapsing that cannot be detected when the value of this scan cell cannot be set to 0 (1) in the launch time frame. As a result, replacing a regular scan cell, which has a large 0 and 1 relative measures, with an enhanced scan cell can create do not care bits in large numbers of test patterns.

The above presented approaches use the full scan to test delay faults. However, the full scan has a performance overhead that cannot always be tolerated for every flip-flop. When certain flip-flops (typically on critical paths) are not modified into scan flip-flops, the result is a partial scan circuit. The partial scan, which was quite popular to test stuck-at faults, is not so popular to test delay faults [14]. Typically, a large percentage of the flip-flops are scanned, resulting in a partial scan circuit with a very high level of scan. Pomeranz and Reddy [14] proposed to scan in values not for all the flip-flops of the scan chain. The unscanned flip-flop have unknown values. But additional patterns are required to bring the circuit from a partially-specified scan-in state to a state where faults can be activated, and to propagate fault effects from unscanned flip-flops. Among these patterns one pattern only is applied under a fast clock, all the other patterns are applied at slow clock.

Conventionally, the scan chain is formed at the gate level, converting the flip-flops into the scan flip-flops depending on the methodology used either full or partial scan. But this approach suffers of: (1) high area overhead added per flip-flop and (2) long test application time due to the serial shifting of test patterns through the scan chain. Obien et al. suggested forming a scan [15] at the register transfer level (RTL) of the circuit. The approach is called F-scan, which organizes F-paths for scan by maximizing use of available functional logic. Each F-path starts with a primary input and ends with a primary output. The approach was improved in [16]. Obien and Fujiwara [16] proposed a hybrid model of the F-scannable circuit for delay automatic test pattern generator that achieves high delay fault coverage. The difference between full scan and F-scan is that while full scan augments multiplexers to connect flip-flops, F-scan exploits available functional elements and paths, hence resulting to lesser area overhead. The test vectors are allowed to be functionally scanned-in and -out of the registers along the F-path given that the side inputs to the functional units are constants. F-paths also allow scan-in and scan-out test vectors simultaneously, thus, similar to full scan, only one test pin is needed to activate scan.

Delay test patterns can be generated even at the higher level of abstraction than RTL [17]. It is a functional level using a software prototype model, with a diversity of black box models, for the cases when the primary inputs, the primary outputs and the state variables are available only. The functional delay fault model was introduced in order to generate test at the functional level using the software prototype model of the circuit [17]. Functional delay test can be constructed for scan and non-scan sequential circuits