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Pass transistor with dual threshold voltage domino logic design using standby switch for reduced subthreshold leakage current ☆

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ABSTRACT

Dual threshold voltages domino design methodology utilizes low threshold voltages for all transistors that can switch during the evaluate mode and utilizes high threshold voltages for all transistors that can switch during the precharge modes. We employed standby switch can strongly turn off all of the high threshold voltage transistors which enhances the effectiveness of a dual threshold voltage CMOS technology to reduce the subthreshold leakage current. Subthreshold leakage currents are especially important in burst mode type integrated circuits where the majority of the time for system is in an idle mode. The standby switch allowed a domino system enters and leaves a low leakage standby mode within a single clock cycle. In addition, we combined domino dynamic circuits style with pass transistor XNOR and CMOS NAND gates to realize logic 1 output during its precharge phase, but not affects circuits operation in its evaluation and standby phase. The first stage NAND gates output logic 1 can guarantee the second stage computation its correct logic function when system is in a cascaded operation mode. The processing required for dual threshold voltage circuit configuration is to provide an extra threshold voltage involves only an additional implant processing step, but performs lower dynamic power consumption, lower delay and high fan-out, high switching frequencies circuits characteristics. SPICE simulation for our proposed circuits were made using a 0.18 μm CMOS process from TSMC, with 10 fF capacitive loads in all output nodes, using the parameters for typical process corner at 25 °C, the simulation results demonstrated that our designed 8-bit carry look-ahead adders reduced chip area, power consumption and propagation delay time more than 40%, 45% and around 20%, respectively. Wafer based our design were fabricated and measured, the measured data were listed and compared with simulation data and prior works. SPICE simulation also manifested lower sensitivity of our design to power supply, temperature, capacitive load and process variations than the dynamic CMOS technologies.

1. Introduction

As the demand for higher performance CMOS VLSI processors with increased complications, we need to improve the performance, area efficiency, and functionality of arithmetic circuits [1]. One of the challenges in VLSI processor design today is to structure multilevel carry look-ahead adders (CLAs) [2,3] circuits specifically for the 8-bit CLA circuits without limiting the functional flexibility. The major tradeoff of these prior gigahertz logic circuits is the high power consumption which is not a tolerable price to pay in recent mobile technologies, these circuits unavoidably consume power even if they are in a standby condition. Since use of the CLA principle for high speed arithmetic units remains dominant, many efforts have been focused on the improvement of CLA design [4,5]. A low power high performance circuit technique was proposed in [5–8] for reducing power dissipation and diminishing propagation delay by feed through dynamic CMOS logic structure. Wang and Tsai [9–11] employed the all-N-transistor dynamic logic blocks to constructed 8-bit CLA which are arranged in a programmable logical array (PLA)-like manner and synchronously triggered. It is implemented on silicon to verify the power reduction as well as the preservation of high speed. The major advantage of this low power design methodology is that it is robust regardless of long data words, e.g., 64-bit binary data. In this paper, we propose a low power high performance CLA circuits structure using modified dual threshold voltage (dual-V_{th}) domino logic blocks [12,13], SPICE simulation shown that our proposed dual-V_{th} domino dynamic logic circuits reduced power consumption more than 45% when compared to the prior works.

Some previous research work results are reviewed in Section 2, previously published leakage control techniques applicable to dual-V_{th} domino logic circuits are also discussed in Section 2. The operation of our proposed standby switch dual-V_{th} domino logic circuit technique is described in Section 3. CLA designed

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based on our proposed dual-V_{th} domino logic cells is presented in Section 4, subthreshold leakage current versus threshold voltage is analysis in Section 5. Simulation and fabrication wafer (chips) measurement results characterizing the standby leakage energy, active mode power and delay of the standby switch technique which are compared to previous works are presented in Section 6. Some conclusions are provided in Section 7.

2. Previous works

Domino CMOS [14–16] logic circuit techniques are extensively applied in high performance microprocessors due to the superior speed and area characteristics when compared to the standard fully complementary static CMOS logic [17,18]. However, the major drawback with the domino dynamic logic circuit is its excessive power dissipation due to the switching activity and the clock load, domino dynamic logic's performance are also mainly affected by charge sharing and race problems. To deal with the excessive power dissipation of the domino dynamic logic, the current design methodologies trade power and critical delay for performance is mainly achieved through a mixture of dynamic and static circuit styles, use of dual supply voltages and dual-V_{th} transistors. Several dual-V_{th} techniques were proposed for reducing standby power dissipation while still maintaining high performance in static and dynamic combinational logic blocks [19,20]. Kao et al. [21] employed dual-V_{th} transistors in domino logic circuits for reducing its subthreshold leakage energy consumption, as shown in Fig. 1(a) in which the high threshold voltage (high-V_{th}) transistors are represented by a thick line in its channel region. The technique proposed in [21] utilizes both high and low threshold voltage (low-V_{th}) transistors, high-V_{th} transistors are employed on the noncritical precharge paths, alternatively, low-V_{th} transistors are employed on the speed critical evaluation paths. However, the circuit technique proposed in [21] does not addressed energy and delay overhead for entering and leaving its standby mode. In order to justify the use of additional circuitry to place a dual-V_{th} circuit into a low leakage state, the total energy consumed to enter and leave the standby mode must be significantly less than the savings leakage energy in the standby mode. Dual-V_{th} domino logic circuit techniques with differently standby mode control mechanisms, i.e., circuit techniques to place a domino logic circuits into a low leakage state regardless of the input vector and the initial circuits node voltage states(before the clock is gated) have been proposed in the literature [22–24]. Kursun et al. [22,23] employed sleep switches to place an idle mode dual-V_{th} domino logic circuit into a low leakage state with low energy and delay overhead, and enters and leaves the standby mode within a single clock cycle, as shown in Fig. 1(b), circuit technique in [22] shown that the sleep switch circuit technique reduces the leakage energy by up to 830 times and dual-V_{th} CMOS technology lowers the subthreshold leakage energy by up to 714 times as compared to a standard low-V_{th} domino circuit for an 8-bit domino CLAs.

However, the circuit output of Fig. 1(b) will be logic 0 during its precharge phase which will cause the second stage cannot evaluate the function itself in its evaluation phase as in a typical two stage dual-V_{th} domino logic circuit to construct a pipeline structure, as shown in Fig. 2. To resolve such a difficulty, Wang et al. [24] proposed a modified dual-V_{th} domino logic circuit, as shown in Fig. 3(a), a clock-controlled nMOS transistor, n22 is inserted in the discharging path of the output inverter for hold circuits output data during its percharge phase, however SPICE simulation shown that the circuit output in Fig. 3(a) has neither charging path nor discharging path in its precharge phase, since when operation clock (clk) gated low (clk=0), p11 is on, n11 and n22 are both switched off, so node A is precharged by p11 to VDD

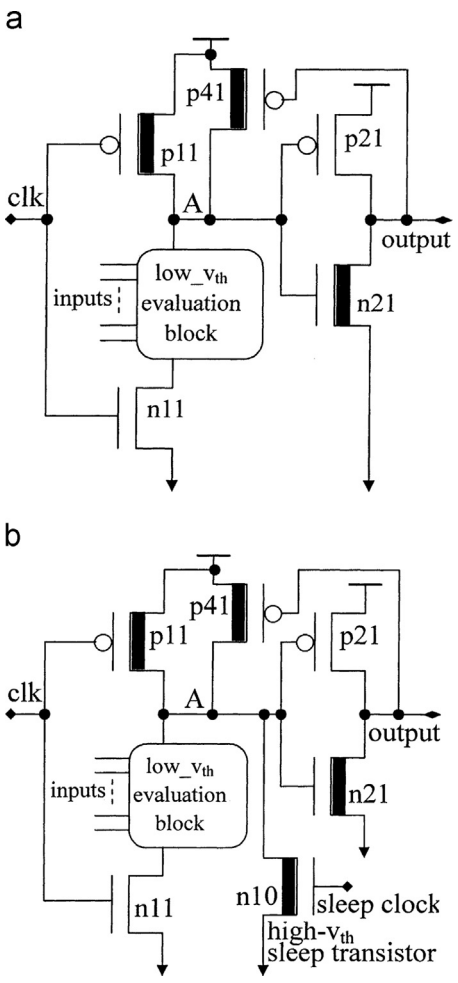

Fig. 1. (a) Typical dual-V_{th} domino logic circuit. The low-V_{th} transistors are represented by standard symbols, high-V_{th} transistors are symbolically represented by a thick line in the channel region. (b) Sleep switch dual-V_{th} domino logic circuit techniques.

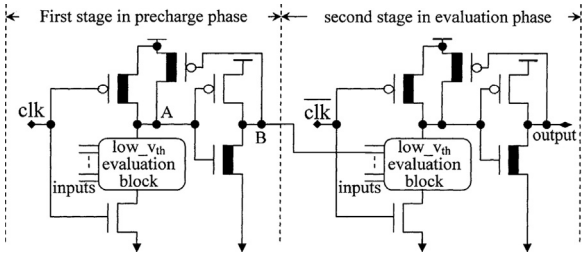

Fig. 2. Typical two-stage dual-V_{th} domino logic circuit to construct a pipeline structure.

which is system supply voltage, thus, p21 is switched off, so that the circuits output is a tri-state not keeping the previous state as described in [24].

3. Proposed standby switch dual-V_{th} domino logic circuits

In order to deal with the difficulty of previous circuits configuration, a low energy and delay overhead dual-V_{th} circuits scheme which employs standby switch to place a dual-V_{th} domino logic circuit into a low leakage state within a single clock cycle was proposed in this paper to lower the subthreshold leakage currents in its idle mode, as shown in Fig. 3(b), a high-V_{th} standby switch