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A 1.33 μW 10-bit 200KS/s SAR ADC with a tri-level based capacitor switching procedure

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ABSTRACT

A 10-bit successive approximation register (SAR) analog-to-digital converter (ADC) using an energy-efficient tri-level based capacitor switching procedure is presented. The proposed switching procedure achieves 97.66% less switching energy when compared to the conventional method. The number of unit capacitors is reduced by a factor of 4 over that of conventional architecture as well. To make the power consumption of the comparator scale down with respect to the comparison rate, the fully dynamic comparator is used. Moreover, the dynamic logic circuit is implemented to further reduce the power of digital circuits. The ADC is implemented in a 0.18 μm 1P6M CMOS technology. At 1.0-V power supply and 200KS/s, the ADC achieves an SNDR of 60.54 dB and consumes 1.33 μW, resulting in a figure-of-merit (FOM) of 7.7 fJ/conversion-step. The ADC core occupies an active area of only 230 × 400 μm^2.

1. Introduction

Low power is one of the most relevant design concerns for energy-limited applications, such as wireless sensor networks and implantable medical devices. Since ADCs are the key blocks of these systems, it is essential to improve the energy efficiency of the ADC to extend the system's life-span. Successive approximation register (SAR) ADC has found wide applications for its moderate resolution, speed, simple structure, and high energy efficiency [1,2].

In SAR ADCs, the primary sources of power consumption are capacitor arrays, comparator, and digital circuits. With the advancement of technology and supply voltage scaling, the digital power dissipation is becoming lower. The fully dynamic comparator is often used owing to its good power efficiency. Therefore, the power of capacitor arrays dominates the overall power consumption of SAR ADCs. Reducing the capacitance of the unit capacitor is an effective way to minimize the power consumption of capacitor arrays. However, using a small unit capacitor will degrade the linearity of ADC because of mismatch issue. Recently, several energy-efficient switching schemes have been developed to reduce the power of capacitor arrays. Compared to conventional architecture [3], the energy-saving [4], monotonic [5], and V_{CM}-based [6] reduce 56%, 81%, and 87.54% switching energy, respectively. In this paper, a more energy-efficient tri-level based capacitor switching procedure is proposed. By using the level shifting technique after the MSB is determined and monotonic switching procedure for subsequent bit steps, the switching energy and number of capacitors have been significantly reduced.

This paper presents a power-efficient SAR ADC that combines several techniques to achieve low power design. First, a novel tri-level based capacitor switching procedure is developed to reduce the power of capacitor arrays. Second, the fully dynamic comparator is adopted to make the power consumption of the comparator scale proportional to the comparison rate. Finally, the dynamic logic circuit is implemented to further reduce the power dissipation of digital circuits. The post-layout simulation results show the ADC achieves an ENOB of 9.76 bit at a sampling rate of 200KS/s. It consumes only 1.33 μW from a 1.0 V supply and achieves a figure of merit of 7.7 fJ/conversion-step.

2. SAR ADC architecture

2.1. Tri-level based capacitor switching procedure

SAR ADCs usually use a binary-weighted capacitor array rather than a C–2C capacitor array or capacitor array with a scaling capacitor for better linearity. Fig. 1(a) and (b) show a conventional differential 10-bit SAR ADC and the proposed SAR ADC, respectively. A differential architecture is employed to have a good common-mode noise rejection and achieve high accuracy. Compared to conventional structure, the proposed ADC reduces the number of

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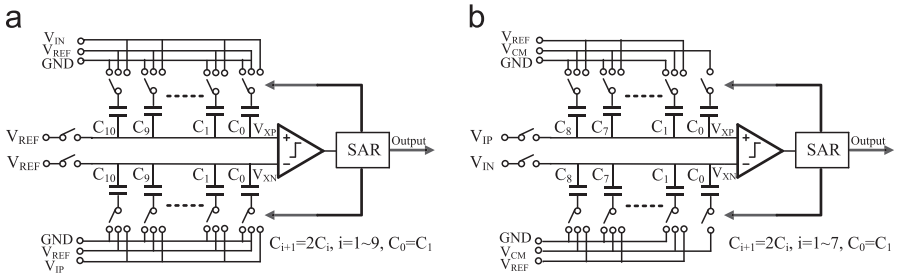

Fig. 1. (a) A conventional 10-bit SAR ADC (b) the proposed SAR ADC architecture.

capacitors by a factor of 4 but requires a third reference voltage V_{CM} which is designed to 1/2 V_{REF}. The operation of the proposed ADC is described below. At the sampling phase, the differential input signal is sampled on the top-plates of two capacitor arrays via sampling switches, and simultaneously the bottom-plates of capacitors are connected to the common-mode voltage V_{CM}. Next, the sampling switches are open and the comparator performs the first comparison without consuming any switching energy. Once the MSB is obtained, the bottom-plates of the capacitor array which samples the higher input voltage are reconnected to ground and the other capacitor array remains unchanged. Thus, the voltage of capacitors on the higher voltage potential side is level-shifted down by 1/2 V_{REF}. The capacitor array consumes no switching energy in this operation. After the MSB comparison, the different reference voltages will be chosen for the differential capacitor arrays, as shown in Table 1. If MSB=1, the positive and negative reference voltages on the V_{XP} side will be V_{CM} and V_{GND}. On the V_{XN} side, the positive and negative reference voltages will be V_{REF} and V_{CM}. Then the ADC performs monotonic switching procedure for the following successive approximation operation which is similar as the scheme in Ref. [5]. According to the comparator output, the largest bit-capacitor C_8 on the lower voltage potential side is switched from V_{CM} to V_{REF} or from ground to V_{CM} and the other bit-capacitor (on the higher voltage potential side) remains unchanged. Then the comparator begins the next comparison. The ADC repeats the producer until the LSB is decided. During the monotonic switching procedure, the proposed scheme only switches one capacitor for each bit cycle, resulting in less switching activity and lower energy. The successive approximation wave for the proposed switching scheme is shown in Fig. 2.

2.2. Switching energy

To further explain the proposed switching scheme, a 3-bit differential SAR ADC as shown in Fig. 3 is used. The quantitative energy consumption of each switching phase for all possible conversions is also shown in the figure. For the proposed switching scheme, the comparator performs the first comparison without consuming any switching energy. After the MSB is determined, the voltage of capacitors on the higher voltage potential side is level-shifted down by 1/2 V_{REF}. As a result, the 2nd-MSB can be decided. There is no energy consumed in this step as the charge-redistribution is completely passive. Then the ADC performs monotonic switching procedure for the subsequent successive approximation operation.

For an N-bit SAR ADC using the proposed switching scheme, if each digital output code is equiprobable, the average switching energy can be derived as

$$E_{avg,tri\_level} = \sum_{i=1}^{N-2} (2^{N-i-5}) CV_{REF}^2 \quad (1)$$

Table 1
Different reference voltages are chosen for differential capacitor arrays according to first comparison result.

Differential input	MSB=1		MSB=0	
	Positive side	Negative side	Positive side	Negative side
Positive reference	V_{CM}	V_{REF}	V_{REF}	V_{CM}
Negative reference	V_{GND}	V_{CM}	V_{CM}	V_{GND}

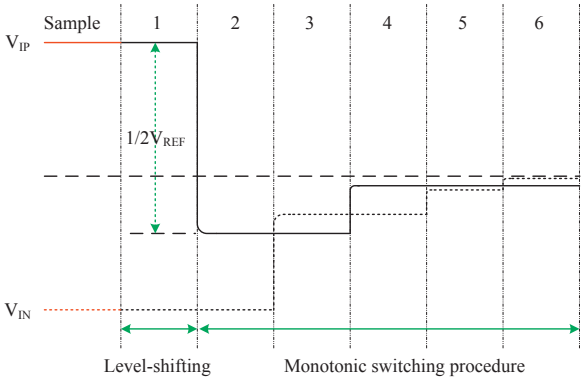

Fig. 2. Waveform of proposed switching scheme.

The average switching energy for an N-bit conventional SAR ADC can be expressed as [5]

$$E_{avg,conv} = \sum_{i=1}^{N} 2^{N+1-2i}(2^i-1) CV_{REF}^2 \quad (2)$$

The average switching energy for a 10-bit conventional SAR ADC is $1365.3CV_{REF}^2$ while the average switching energy for a 10-bit SAR ADC using the proposed switching scheme is only 31.88 CV_{REF}^2. The proposed scheme achieves 97.66% switching energy saving with respect to the conventional one. Energy saving [4] and monotonic switching [5] schemes provide only 56% and 81% reductions, respectively. A comparison of switching energy for the reported switching schemes versus the output code is shown in Fig. 4.

2.3. Linearity

The unit capacitor in the SAR ADC capacitor array is typically limited by matching requirements. Assuming the unit capacitor is modeled with a nominal value of C_u and a standard deviation of σ_u. For the conventional switching scheme, the mid-code transition is considered as the worst case, since at this transition, all the capacitors change their state. A conventional differential N-bit binary-scaled DAC is composed of $2 \times 2^N C_u$-elements, with an LSB step of $2C_u$ (the factor of 2 arises from the differential implementation) [7]. At the MSB code transition all capacitors are switched,