Microelectronics Journal ∎ (∎∎∎∎) ∎∎∎–∎∎∎

Contents lists available at ScienceDirect

Microelectronics Journal

journal homepage: www.elsevier.com/locate/mejo

A low-power, temperature and supply voltage compensated current starved ring oscillator

Niko Bako*, Adrijan Baric

University of Zagreb, Faculty of Electrical Engineering and Computing, Unska 3, 10000 Zagreb, Croatia

ARTICLE INFO

Article history:
Received 30 April 2013
Received in revised form
24 July 2013
Accepted 26 July 2013

Keywords:
Oscillator
Temperature compensated frequency
Supply voltage compensated frequency
Low-power

ABSTRACT

A low-power, 3.82 MHz oscillator based on a feedback loop is presented. The oscillator does not need a stable current reference to obtain a stable frequency independent of voltage and temperature variations because of the usage of negative feedback. The frequency variation, in the temperature range from −20 °C to 80 °C, is ± 0.6% and it depends only on the temperature coefficient of the resistor *R*, while the reference current variations are −11%/+25% in the same temperature range. The oscillator power consumption is 5.1 μW and the active area is 0.09 mm^2. The proposed oscillator is implemented in a 0.18 μm CMOS process and the simulation results are shown.

1. Introduction

A low power oscillator is a circuit specially required for low-power sensor networks, RFID applications and biomedical applications. The most important parameter of the oscillator is the frequency stability over temperature and voltage variations. Besides the frequency stability, the oscillator must be capable to operate at low supply voltages and maintain low power consumption. Oscillators for RFID applications are mostly relaxation oscillators because this type of oscillators is capable to operate at very low voltages (e.g. 0.8 V and 0.6 V in [1,2]) and have very low-power consumption (very often hundreds of nanowatts) [1–4]. However, the oscillation frequency depends on transistor thresholds, the timing capacitor, and the reference current for charging and discharging the time capacitor which result in variations of the oscillation frequency over PVT [1]. The frequency stability of the relaxation oscillators, implemented as a cross-coupled *RC* multivibrator, depends on a voltage swing across the cross-coupled capacitor. The voltage swing depends on transistor parameters (e.g. threshold voltage) so it must be PVT compensated in order to achieve a stable frequency [2]. The examples of oscillators for sensor nodes and biomedical devices are presented in [5,6]. The key idea behind these oscillators is to employ a feedback for frequency regulation of the VCO. Because of the feedback, the frequency depends only on the capacitance *C*, regulated (PVT independent) voltage and current references, but not on the transistor threshold voltages. The drawback of this approach is a larger consumption (compared with the relaxation oscillator).

In both types of the above described oscillator topologies a stable reference current, independent of the supply voltage and temperature variations, is essential to obtain a stable oscillator frequency. However, it is very hard to achieve a stable current in a wide temperature range although there are examples of the current starved VCOs with very stable current references (e.g. [7]). Besides, current variations depend on the technology (process) in which the current reference is designed (for the same technology node the current variations will be different for different processes). This paper proposes an oscillator topology based on feedback which does not need a stable current reference to obtain stable oscillation frequency.

The paper is structured as follows. Section 2 presents the oscillator architecture, Section 3 the oscillator performance and Section 4 brings conclusion.

2. Oscillator architecture

The oscillator architecture, which employs the negative feedback for stabilization of the VCO frequency, is shown in Fig. 1. It consists of a low power current–voltage reference circuit, comparator (operational amplifier), voltage controlled oscillator (5-stage current starved ring oscillator, VCO), frequency divider and frequency-to-voltage converter (FVC) [8]. The FVC input is the signal that has the frequency equal to the output frequency divided *M* times and the output is the voltage V_{FVC}. In addition to the frequency, the voltage V_{FVC} depends also on the current I_{FVC}.

* Corresponding author. Tel.: +385 1 6129 547.
E-mail address: niko.bako@fer.hr (N. Bako).

0026-2692/$ - see front matter © 2013 Elsevier Ltd. All rights reserved.
http://dx.doi.org/10.1016/j.mejo.2013.07.004

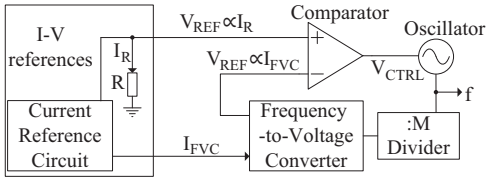

Fig. 1. Block scheme of the oscillator.

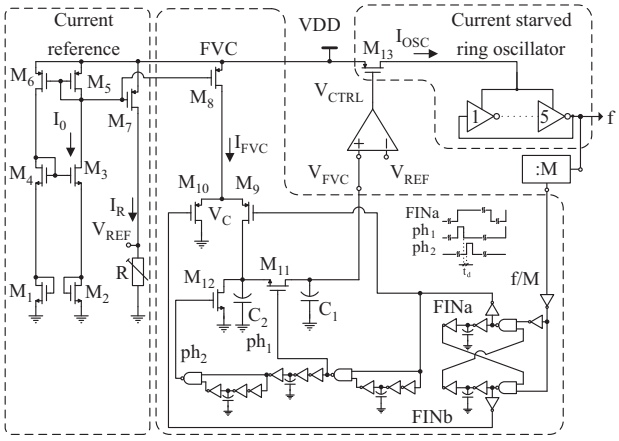

Fig. 2. Circuit level implementation.

Together with the divider, the FVC circuit forms a negative feedback loop. The loop is locked when the reference voltage V_{REF}, which is proportional to the current I_R, is equal to the voltage V_{FVC} at the FVC output. The operational amplifier forces $V_{REF}=V_{FVC}$ by changing the oscillator frequency. The idea is to make both V_{REF} and V_{FVC} proportional to the currents I_R and I_{FVC} which are generated in the same *I–V* reference circuit. Since $V_{REF}=V_{FVC}$, the current variations will cancel each other and the oscillator frequency will be stable and independent of the current variations. The circuit level implementation is shown in Fig. 2.

In Fig. 2 the transistors M_1–M_6 form the current reference circuit based on [9]. The reference circuit generates the currents I_R and I_{FVC} for the voltage reference V_{REF} and for the FVC circuit. The transistors M_3 and M_4 operate in subthreshold region and M_1 and M_2 operate in strong inversion and saturation [9]. The current I_0 is given by [9]

$$I_0 = \frac{m^2 V_T^2 k_2}{2}\left(\frac{N}{N-1}\right)^2 \ln^2\left(\frac{W_3/L_3}{W_4/L_4}\right) \tag{1}$$

where $N=\sqrt{k_1/k_2}$ ($k=k_n' W/L$), k_n' is nMOS transconductance parameter in saturation, V_T is the thermal voltage and m is the subthreshold swing parameter. The current I_0 generated by the circuit may not be accurate and stable over PVT variations, but it has to be as low as possible because of the power consumption of the reference circuit. I_0 is mirrored and delivered to the rest of the oscillator circuitry (operational amplifier, FVC and VCO) so the current must be as low as possible. The targeted current is 100 nA at room temperature, what is close to the obtained simulated current of 106 nA. Fig. 3 shows I_0 stability over temperature variations. The current varies 15% with respect to the current at room temperature.

The transistors M_7 and M_8 are matched and implemented as multiple parallel transistors (e.g. each transistor consists of parallel units) so that $I_{FVC}=nI_R$ (n is calculated as: (number of parallel units of M_8)/(number of parallel units of M_7)). The current I_R is converted into the reference voltage V_{REF} on the resistor R ($V_{REF}=I_R R$).

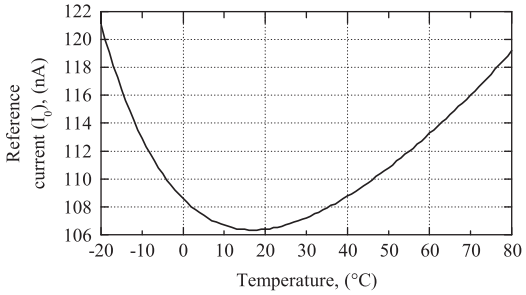

Fig. 3. Simulated stability of the current I_0 over temperature variations.

The FVC circuit from [8] is shown in Fig. 2. The circuit consists of the non-overlapping clock generator which generates the signals *FINa*, *FINb*, ph_1 and ph_2, two capacitors (C_1 and C_2) and transistors M_8–M_{12}. The input of the FVC circuit is the frequency f and the output of the circuit is the voltage V_{FVC}. V_{FVC} is generated in the following way. During the integration half-period T_{INT} the signal *FINa* is set low (*FINb* is set high) and the current I_{FVC} flows through M_9 (M_{10}, M_{11} and M_{12} are off) and charges the capacitor C_2. The voltage on C_2 is

$$V_{C2} = I_{FVC} T_{INT}/C_2. \tag{2}$$

In the second half-period (transfer half-period) M_9 is off (*FINa* is set high) and M_{10} is on (*FINb* is set low). The transistor M_{10} is used to eliminate voltage spikes at the node V_c that can be generated during the switching of the transistor M_9 [8]. The rising edge of the signal *FINa* generates the very short signal ph_1 (ph_1 is set high) so M_{11} is on and the charge stored on C_2 is transferred to C_1 which is the FVC output. Charge transfer ends when ph_1 is set low. High level of ph_1 must last sufficiently long in order to complete the charge transfer from C_1 to C_2. On ph_1 falling edge the non-overlapping clock generates ph_2 which resets the capacitor C_2. It is important that the signals ph_1 and ph_2 are non-overlapping signals so ph_2 is delayed by t_d after ph_1. The necessary minimal (the worst case) t_d obtained by PVT simulations is 100 ns. This concludes the FVC operation in one period (T). The described procedure repeats for each period and the output voltage of FVC (V_{FVC}) refreshes in each transfer half-period. The output voltage is stored in C_1. The oscillator frequency ($f=1/T$) is divided M times and regarding (2) the output voltage V_{FVC} is

$$V_{FVC} = \frac{V_{FVC}' C_1 + V_{C2} C_2}{C_1 + C_2} = \frac{V_{FVC}' C_1 + I_{FVC} C_2 MT/2}{C_1 + C_2} \tag{3}$$

where V_{FVC}' is the voltage stored on C_1 during the previous period. If $C_1=C_2=C$, the absolute error $(V_{FVC}'-V_{C2})/V_{C2}$ is 0.4% after 8 transfer half-periods [8].

In the stable state when $V_{REF}=V_{FVC}$, the feedback loop is locked. When the loop is locked $V_{FVC}'=V_{C2}$ and the output voltage V_{FVC} in the stable state is

$$V_{FVC} = \frac{I_{FVC}}{C} M \frac{T}{2} = \frac{I_{FVC}}{C} M \frac{1}{2f}. \tag{4}$$

The comparator that generates the voltage V_{CTRL} (Fig. 2) is an operational amplifier and it is implemented as a simple Miller compensated operational amplifier (Fig. 4). The proposed oscillator is a circuit with the negative feedback and its stability must be assured. In conventional phase-locked loops (PLLs) a low-pass filter is used to stabilize PLL. The low pass characteristics of the Miller compensated amplifier can be used for stabilization of the oscillator. The bandwidth of the operational amplifier (low-pass filter) is defined by the Miller capacitor (C_c) in the amplifier (Fig. 4). The amplifier has the following characteristics: DC gain is 75 dB, phase margin 80°, current consumption 200 nA and gain-bandwidth product (GBW) is 3.5 kHz. The capacitor of 20 pF is

Please cite this article as: N. Bako, A. Baric, A low-power, temperature and supply voltage compensated current starved ring oscillator, Microelectron. J (2013), http://dx.doi.org/10.1016/j.mejo.2013.07.004