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Hybrid cascode feedforward compensation for nano-scale low-power ultra-area-efficient three-stage amplifiers

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ABSTRACT

A modified frequency compensation technique is proposed for low-power area-efficient three-stage amplifiers driving medium to large capacitive loads. Coined hybrid cascode feedforward compensation (HCFC), the total compensation capacitor is divided and shared between two internal high-speed feedback loops instead of only one loop as is common in prior art. Detailed analysis of this technique shows significant improvement in terms of bandwidth and stability. This is verified for a 1.2-V amplifier driving a 500-pF capacitive load in 90-nm CMOS technology, where HCFC reduces the total capacitor size and improves the gain-bandwidth by at least 30% and 40% respectively, compared to the prevailing schemes.

1. Introduction

Frequency compensation is a conventional design step in the design procedure for negative-feedback amplifiers used in drivers, filters, data converters and low-dropout regulators [1–17]. Depending on the load capacitor (C_L), a minimum compensation capacitor (C_C) is required to maintain stability, by which the gain-bandwidth (GBW) and slew-rate (SR) are affected depending on their value. With two large compensation capacitors proportional to C_L, the well-known nested Miller compensation (NMC) [1–3] fails to achieve sufficient GBW and SR under low power constraints. Various frequency compensation strategies have therefore been proposed to reduce the size of the compensation capacitors with limited power budget. Multipath nested Miller compensation (MNMC) [6] compensation is among these solutions which aims to further push away the power/area envelope. It uses a feedforward stage to implant an additional left-half-plane (LHP) zero to the NMC transfer function. The undesired right-half plane (RHP) zero in basic NMC architecture imposes excessive power for sufficient stability. Nested *Gm-C* compensation is another compensation solution dedicated for three-stage amplifiers to remove this RHP zero [7]. Looking for ways to remove the bulky capacitance used within the internal ac feedback loop of the NMC has also been the idea of some improved architectures. This capacitance is used to control the location of the complex poles for adequate gain margin (GM). The damping-factor-control frequency compensation (DFCFC) [8] replaces this capacitor with an active damping-factor-control unit. As a step further, the main compensation capacitor is substituted with an active capacitance in active feedback frequency compensation (AFFC) [9], resulting in improved stability with lower compensation capacitance. The remaining passive capacitance in AFFC is replaced by a damping-factor-control unit in dual-loop parallel compensation (DLPC) [10]. Two high-speed paths are also included to extend the bandwidth and to reduce the capacitor [10]. A serial RC network is added at the output of the amplifier intermediate stage to create a LHP zero in impedance adapting compensation (IAC) [11]. A standard Miller capacitance is also used for pole-splitting. Combining the concepts of signal feedforwarding and pole-splitting, single Miller capacitor feedforward frequency compensation (SMFFC) successfully removes the second compensation capacitance in NMC topology [12]. As proposed, the sizing of the remaining capacitance can also be decreased when increasing the gain of the intermediate stage [12].

To stabilize the amplifiers driving ultra-large capacitive loads, a few compensation techniques have been reported so far. Among these solutions are single capacitor with current amplifier compensation (SCCAC) [13], and current-buffer Miller compensation (CBMC) plus parasitic-pole cancellation [14,15].

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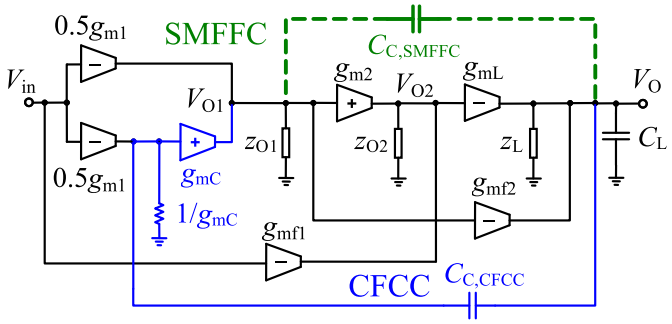

Fig. 1. Block diagram of a three-stage amplifier with SMFFC and CFCC.

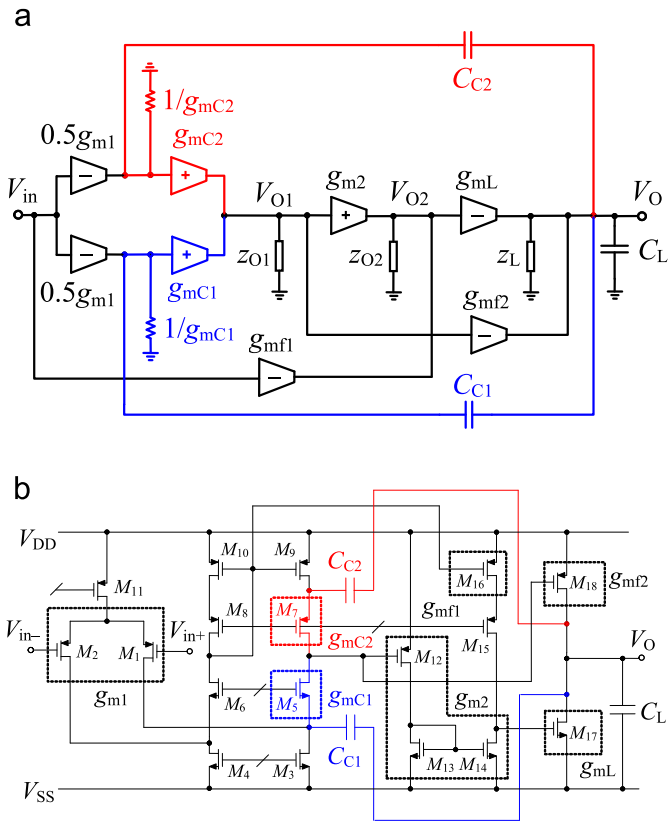

Fig. 2. Structure of a three-stage HCFC amplifier: (a) block diagram; and (b) circuit-level implementation.

The available compensation solutions some of which reported above considerably reduce the size of the compensation network, yet, unless consuming significant power, this block still remains as one of the largest parts of the integrated negative-feedback amplifiers [5–15].

Cross feedforward cascode compensation (CFCC) [16] is one of the recently-proposed effective solutions to decrease the size of the compensation capacitance in a three-stage operational amplifier. In comparison with other topologies based on the required capacitance value, power consumption, and design complexity, it shows better performance metrics for capacitive loads up to a few nano-farads [5–16]. Fig. 1 depicts a three-stage amplifier with one compensation capacitance either in SMFFC or CFCC configurations. Compared to advanced variations of NMC, SMFFC needs less area for implementation as the required C_C is divided by the gain of the intermediate stage [12]. A transconductance (g_m)-stage (g_{mC}) in series with the compensation capacitance further decreases the required area in accordance with the results from CFCC [16]. This makes C_C a function of $\sqrt{C_L}$ rather than C_L in SMFFC that is considerably effective especially for larger capacitive loads.

Coined hybrid cascode feedforward compensation (HCFC), Fig. 2a shows the proposed compensation scheme with two compensation capacitors, i.e., C_{C1} and C_{C2}. A similar compensation scheme proves useful for low-dropout regulators and two-stage operational amplifiers [4,17]. One important observation from this topology is that instead of a single loop to stabilize the amplifier as occurs in Fig. 1, HCFC shares the total capacitance between two high-speed feedback loops each with a corresponding g_m-stage (g_{mC1} and g_{mC2}) [4]. The output current is thus sensed and buffered via g_{mC1} and g_{mC2} simultaneously. For equal g_{mC1} and g_{mC2}, the amount of ac current fedback by the compensation network to the first gain stage is now twice that of CFCC. This decreases the total loading of the compensation network on the output node and, for the same capacitance as CFCC, extends the bandwidth. Hence, identical stability margins are resulted with smaller compensation network and, accordingly, smaller operational amplifier. A circuit-level implementation of a three-stage HCFC amplifier is illustrated Fig. 2b. The additional g_m-stage (g_{mC2}) required in this topology is properly embedded to the input stage without any increase in die size and power.

A few key parameters should be taken into consideration in order to quantify and fairly compare the efficiency of various frequency compensation topologies. Among these variables, the supply current of the amplifier (I_{DD}), the load capacitance it can drive (C_L), and the achieved GBW and SR are especially important. Based on these metrics, the two widely-used figures of merit, IFOMS$=$GBWC_L/I_{DD} and IFOML$=$SRC_L/I_{DD}, can be used to characterize the small-signal and large-signal capabilities. Comparing the results for HCFC with CFCC, the proposed technique improves the small-signal IFOMS and the large-signal IFOML by at least 40%.

The rest of this paper is organized as follows. The proposed HCFC is analyzed based on the transfer function, stability, noise, and slew-rate in Section 2. In Section 3, the HCFC is compared with SMFFC and CFCC from different perspectives from small-signal to large-signal behaviors. As an important result, it is shown that the HCFC can achieve similar stability margins with compensation capacitor values considerably smaller than in SMFFC and CFCC. A proposed HCFC amplifier is detailed and carefully simulated in Section 4. The conclusions are drawn in Section 5 along with a few comments for future works.

2. Hybrid cascode feedforward compensation

2.1. Transfer function

The amplifier diagram in Fig. 2a contains three main gain stages each with an equivalent transconductance (g_{m1}, g_{m2}, g_{mL}), and an output impedance (z_{o1}, z_{o2}, z_{oL}). Each output impedance is composed of a capacitance element (C_{P1}, C_{P2}, C_L) along with a conductance (g_{O1}, g_{O2}, g_L), where $z_{Oi}=1/(g_{Oi}+sC_{Pi})$. The amplifier also contains two feedforward stages (g_{mf1} and g_{mf2}) to improve the large-signal settling response as well as the small-signal settling behavior [8,10,12,16]. Analysis of this topology is simplified (and, as will be shown later, improved) by defining an equivalent transconductance g_{mC} and a total compensation capacitor C_C such that:

$$g_{mC}=g_{mC1}=g_{mC2} \quad \text{and} \quad C_C=2\times C_{C1}=2\times C_{C2}. \tag{1}$$

To obtain a simplified transfer function for this topology, the following assumptions are considered to hold:

(1) The DC gains of all the stages are much greater than unity.
(2) The parasitic output capacitors C_{P1}, and C_{P2} are much smaller than C_C and C_L.

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