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Two dimensional analytical modeling for asymmetric 3T and 4T double gate tunnel FET in sub-threshold region: Potential and electric field

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ABSTRACT

In this paper a two dimensional analytical model of channel potential and electric field for an asymmetric and symmetric double gate three-terminal (3T) and four-terminal (4T) silicon n-tunnel field effect transistor (Si-nTFET) device in sub-threshold region, without surface accumulation or inversion, is presented. Since the modeling has been done in subthreshlod regime operation, no Quantum Mechanical (QM) study has been taken. A very good agreement of analytically modeled results with the TCAD simulated results for the three-terminal (3T) and four-terminal (4T) Si-nTFET device was found. The model presented is based on the physics of the device. The modeling is for a 3T/4T asymmetric Tunnel FET and with appropriate changes in the device parameters we can also model for symmetric devices as well. The modeling scheme is thus quite robust.

1. Introduction

The tunnel field-effect transistors (TFETs) are promising successors of metal-oxide-semiconductor (MOS) FETs [1] due to their potential for sub-60 mV/dec sub-threshold swing [2–4] and very low off current (~femtoamperes) [5]. Such a reduced swing is a necessary requirement for the ultra-low power, ultra-low voltage operation for the next generation of transistors. Other device configurations have been re-evaluated, like the nano-electromechanical (NEM)-based devices, super-steep sub-threshold-slope complementary MOSFETs and other impact ionization-based devices [4]. It can be concluded that the TFET is still the most promising device both due to its strong similarity with the MOSFET configuration, which allows significant re-use of the MOSFET expertise, and due to the absence of reliability issues with the TFET. At the same time, it is recognized that the full potential of the TFET is not yet uncovered and that the ongoing optimization of the TFET configuration is very important. Since the sub-threshold swing of TFET is almost independent on the temperature, hence Tunnel FETs are better candidates at higher temperature applications [6,7], where these can be used as digital switches.

As explained in [8] and [9], high–κ gate dielectrics used for gate will increase the tunnel FET ON current, hence HfO_2 is used as gate dielectric. Double gate (DG) tunnel FETs have the advantages like volume inversion, setting the threshold voltage by the gate work function. There are two main types of DG TFETs: (1) a symmetric type TFET with identical gate work functions, gate oxide material and gate oxide thickness so that the two surface channels turn on at the same applied gate voltage, here *surface channel*, means the channel near the $Si–SiO_2$ interface and (2) an asymmetric type TFET, where there is difference in front gate oxide and back gate oxide in terms of either one or both material or thickness, as a result the tunneling takes place at different applied gate voltages. Further both the above configurations can be applied to three-terminal (3T- when front gate and back gate are tied together) and four-terminal (4T-when front gate and back gate work as two independent terminals) TFET [10,11]. In four-terminal device since the back gate can be adjusted independently, hence the user has the flexibility to set the threshold voltage of the device according to requirement, hence 4T plays significant role in digital circuit design.

This paper is organized as follows: the working principle of TFET is described in the next section, previous work is described in Section 3, analytical modeling is described in Section 4, then results and discussions followed by a conclusion in Sections 5 and 6 respectively.

2. Working principle of TFET

Tunnel Field Effect Transistor is basically a reverse biased p-i-n structure which works on the phenomenon of band to band

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tunneling (BTBT), due to the reverse biased operation, its OFF current is very less (~ femtoamperes) [5].

The DG TFET structure is shown in Fig. 1, here source is degenerately doped with boron concentration of 10^{20} atoms/cm^3 and the drain is doped with phosphorus concentration of 5×10^{18} atoms/cm^3 are heavily doped while channel is near intrinsic with boron doping of 10^{17} atoms/cm^3 [9,12,13]. Here channel is p-type doped, same as given in reference [13], because if we make it lightly n-type doped then it will cause the channel region energy band diagrams to pull downwards in Fig. 2a, hence even at $V_{gs}=0$ V, tunneling of electrons will take place at source-channel junction that will cause to increase the OFF state TFET current. In case of n-TFET, electrons from top of the valence band of p^+ source tunnel to the conduction band of the channel region and tunneling current flows. How it happens is described below.

As shown in Fig. 2a, for $V_{ds}=1$ V and $V_{gs}=0$ V, valence band of the source is not aligned with the conduction band of the channel, hence there is a small probability of tunneling and the current due to tunneling will be small, as shown in Fig. 4, as $\sim10^{-17}$ A/μm.

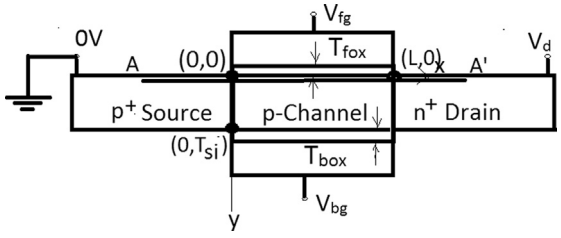

Fig. 1. Double gate n-TFET structure.

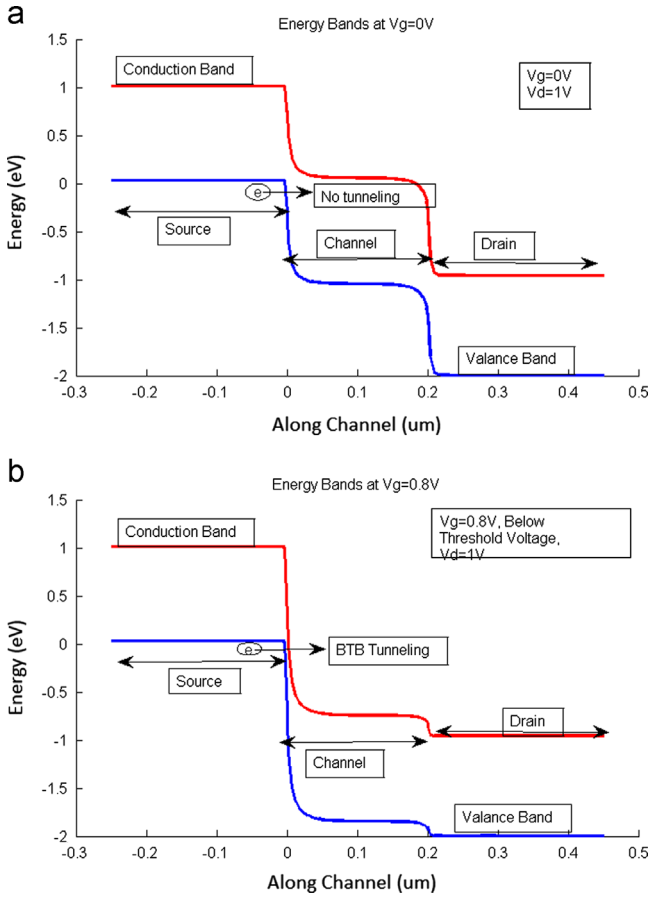

Fig. 2. Energy band diagrams along AA′ cut in Fig. 1, at $V_{ds}=1$ V, $V_{gs}=0$ V and 0.8 V respectively: (a) energy band diagrams along AA′ cut (Fig. 1), at $V_g=0$ V and (b) energy band diagrams along AA′ cut (Fig. 1), at $V_g=0.8$ V.

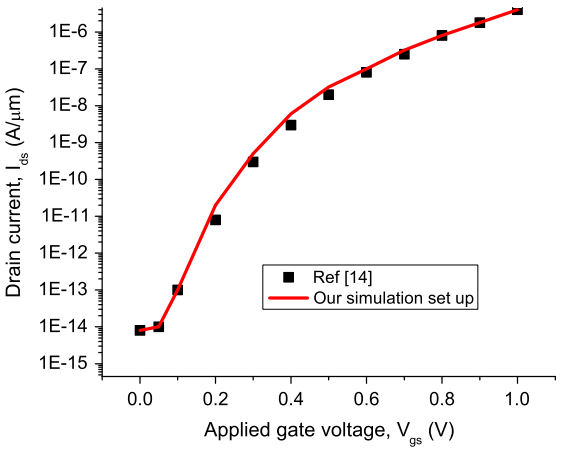

Fig. 3. $I_{ds}-V_{gs}$ calibration with the previously reported work in [14], for this calibration all physical dimensions are used from [14] and then the tuning for carriers' effective masses and life times is done to calibrate the results.

As the applied gate voltage is increased the conduction band of the channel goes well below the valence band of source and the effective BTBT distance reduces near the source/channel interface there by increasing the probability of charge tunneling into the channel region, as shown in Fig. 2b, in this way tunneling probability and therefore tunneling current increases.

There is qualitatively and quantitatively good agreement between our model and simulated data using TCAD Sentaurus. The model results are also matched with previously reported work in [12].

2.1. Simulation set up

The simulation set up used in Sentaurus TCAD is calibrated against the previously reported data in [14], which is already calibrated against experimental data reported in [15]. For this purpose a device is prepared for simulation with dimensions as shown in [14]. Since the flat part of the $I_{ds}-V_{gs}$ curve is due SRH recombination, therefore the carrier life times have been tuned in this part calibration. Rest of the curve is due to band to band tunneling for which we have used WKB approximation and effective masses of carriers have been tuned to calibrate this part. The calibrated results are shown in Fig. 3, in this case we have used the gate metal with work function 4.05 eV.

For subsequent work, we have used the calibrated model file while the physical dimensions and work functions have been changed to show the robustness of the model.

3. Previous work

Lee et al. have developed a potential model for SG TFET in sub-threshold region [16], but they have consider the channel region as intrinsic region, and source-drain regions are heavily doped. If source-drain regions are heavily doped (say 10^{20} atoms/cm^3), in that case in order to avoid convergence problems the channel region at least should be doped at 10^{16} atoms/cm^3 which is very much larger then the intrinsic doping value.

Bardon et al. have analytically modeled surface potential, electric field and drain current for double gate symmetric Si-tunnel FET [12]. The author assumed initially parabolic solution for the symmetric double gate, so there is no flexibility to change the device parameters independently. The author has used conformal mapping directly, but has not changed the limits accordingly.

Tunnel field-effect transistors (TFETs) are potential successors of metal-oxide-semiconductor FETs because scaling the supply

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