Microelectronics Journal 44 (2013) 1285–1289

Contents lists available at ScienceDirect

Microelectronics Journal

journal homepage: www.elsevier.com/locate/mejo

A low-power differential injection-locked frequency divider with output power flatness in 0.5 μm E/D-mode GaAs PHEMT

Fan-Hsiu Huang [a,*], Yue-Ming Hsin [b]

[a] Department of Electronic Engineering, Chang Gung University, Kweishan 333, Taiwan
[b] Department of Electrical Engineering, National Central University, Jhongli 320, Taiwan

ARTICLE INFO

Article history:
Received 19 August 2012
Received in revised form
23 August 2013
Accepted 27 August 2013
Available online 18 September 2013

Keywords:
Enhancement/depletion-mode PHEMT
Injection locking
Frequency divider

ABSTRACT

This study implemented an injection-locked frequency divider (ILFD) on *Ka*-band millimeter-wave communication systems in 0.5 μm enhancement/depletion-mode (E/D-mode) GaAs PHEMT technology. The ILFD presents a low-power design based on the differential-injection circuit topology without using any injectors. Compared with the conventional single-injection ILFD circuits, the proposed ILFD exhibits output power flatness and wide locking range characteristics with a power consumption of 0.9 mW under a 0.4 V supply. The self-oscillation frequency was chosen to be 20 GHz for divided-by-2 operation. The measured locking range is approximately 11.5 GHz ranging from 32.5 GHz to 44 GHz when the injection power level is 5 dBm. The locking range exhibiting a 3 dB power roll-off characteristic at output is 10.5 GHz ranging from 33 GHz to 42.5 GHz.

1. Introduction

A frequency divider/prescaler is an essential sub-circuit to perform frequency division and timing synchronization in microwave/millimeter-wave phase-locked loop (PLL) or clock/data recovery (CDR) circuits. To achieve high-speed and low-power performance without using a complicated circuit topology in such applications, the injection-locked frequency divider (ILFD), based on an oscillator, is a favorable approach [1–7]. The ILFD using differential injection has also been used for quadrature signal generation [1,2]. However, the locking range performance under high-frequency operation is always a major concern because the quality factor (Q), nonlinear coefficients, and amplitudes of the injected and output signals influence the injection efficiency. To overcome the locking-range obstacle, single-injection ILFD using inductor/transformer compensation or the reduced-*Q* technique to enhance the injection efficiency has been reported in [3–5]. In addition, ILFD usually exhibits a sharp drop in output-versus-frequency characteristic because the injected frequency is varied at a low supply voltage, depending on the amplitude of the injected signal and the input–output phase difference. This predicament results in a serious sensitivity degradation and low operation frequency range if the frequency dividers are utilized in series. An ILFD with an output power flatness characteristic, therefore, must be achieved to alleviate the problem. In this paper, we propose a differential-injection ILFD to achieve a wide locking range and a low variation in an output power characteristic. The proposed ILFD was designed without using a direct- or tail-injector to reduce the parasitic effect or voltage drop from the injectors. The circuit topology of the design can be applied to applications of differential type integrated circuits.

2. Injection-locked frequency divider circuit description

The circuit diagram of the proposed differential-injection ILFD is shown in Fig. 1. The ILFD circuit was designed and fabricated using *WIN* 0.5 μm E/D-mode PHEMT technology. To be an injection-locked frequency divider with differential injection, a self-oscillation oscillator must first be conducted. The free-running frequency in the oscillator is chosen to be 20 GHz for divided-by-2 operation. The ILFD consists of two enhanced-mode PHEMTs (M_1 and M_2), transmission-line resonators (TL_1 and TL_2), broadband balun, and spiral inductors (L_1 and L_2). The gate width of the transistor is 25 μm in a two-finger layout. The cutoff frequency (f_T) and maximum oscillation frequency (f_{max}) of the PHEMTs are approximately 45 GHz and 70 GHz under a 1 V supply, respectively. To further reduce the influence from the injectors in conventional ILFDs, such as the voltage drop, parasitic effect, and the injection efficiency, we propose a circuit topology using direct injection through nodes *A* and *B*. Here, L_1 and L_2 have small voltage drops due to the low resistance in the low frequency operation, but the characteristic of the inductors turns into high impedance at high frequencies to isolate the RF-to-DC path. The injected signals, therefore, can be fed into the oscillator without signal leakages through L_1 and L_2. The differential signal is injected at

* Corresponding author. Tel.: +886 3 2118800x5795; fax: +886 3 2118700.
E-mail address: fshuang@mail.cgu.edu.tw (F.-H. Huang).

0026-2692/$ - see front matter © 2013 Elsevier Ltd. All rights reserved.
http://dx.doi.org/10.1016/j.mejo.2013.08.017

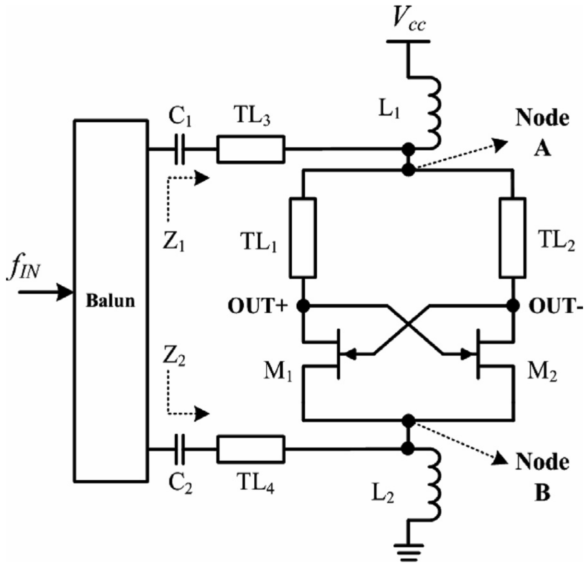

Fig. 1. Schematic diagram of the differential-injection ILFD.

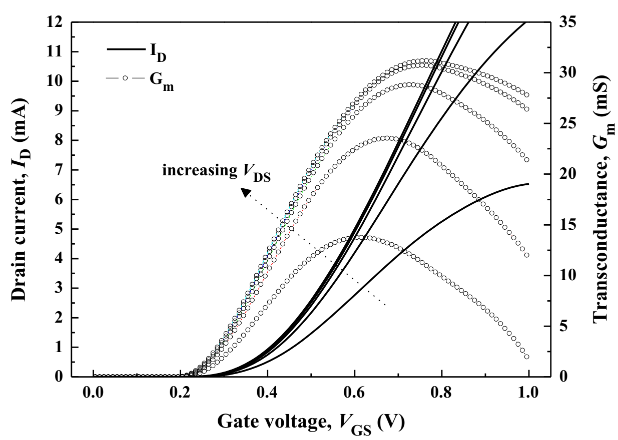

Fig. 2. Drain current (I_D)/transconductance (G_m) characteristics versus gate and drain biases (V_{DS}=0.2 V~1 V, step 0.2 V).

nodes *A* and *B* through the balun. The simulated input impedances, Z_1 and Z_2, are approximately 50 Ω to achieve a low return loss characteristic at 40 GHz. By adjusting C_1, C_2, TL_3 and TL_4, the simulated input impedances, Z_1 and Z_2, can present a broadband matching characteristic.

To further explain how the circuit can be operated at such low voltage, DC and RF characteristics of HEMT transistor are exhibited as follows:

Fig. 2 shows the curves of drain current (I_D) and transconductance (G_m) of HEMT device (2 × 25 μm), where the solid lines are the performances I_D, and dot lines are the characteristics of G_m. The gate bias V_{GS} is varied from 0 V to 1 V with driving drain bias V_{DS} ranging from 0.2 V to 1 V, where the voltage step is 0.2 V. It is clear that an increasing V_{DS} indeed carries out a high current slope and a high G_m performance when V_{GS} is driven over 0.5 V, and the threshold voltage is close to 0.3 V. The curves also indicate that the low variation values in I_D and G_m can be achieved if the bias V_{DS} is set over 0.4 V. In order to a low voltage operation for the proposed circuit, the drain bias V_{DS}=0.4 V was be chosen. Additionally, L_2 presents a low resistance at DC operation as shown in Fig. 1. A particular bias point, $V_{DS}=V_{GS}$=0.4 V, is therefore determined owing to the cross-coupled circuit topology. For such bias point, I_D current is 750 μA with G_m value of 11 mS.

After establishing the bias point, an impedance analysis for cross-coupled circuit is used to reveal that the circuit can satisfy the oscillation condition at a chosen frequency [8]. Fig. 3 exhibits the real part of *Z* parameter versus test frequency depending on different V_D biases. It is evident that a negative resistance will be generated when bias V_{DS} is driven over 0.4 V. A high V_{DS} also presents a wide frequency range within more negative resistance. In order to give consideration to high operating frequency and low dc power consumption in the circuit design, a proper oscillation frequency here is determined around 20 GHz under the bias voltage $V_{DS}=V_{GS}$=0.4 V according to DC analysis. In the simulation, the oscillator can successfully get into an oscillation state with including the passive components of TL_1, TL_2, L_1 and L_2.

The injection locking phenomenon in an oscillator, such as the locking range and output power, has been investigated using the behavioral feedback model, as shown in Fig. 4 [1]. The model is built by a nonlinear mixer and a bandpass filter (BPF), $H(\omega)$, where the injected and frequency-divided signals are presented as $I_{DC}+I_{RF}$ (ω_I) and V_o (ω_o), respectively. The nonlinearity of the differential pair is presented as the nonlinear mixer, where an injector is involved in the mixer. The frequency transfer response causing an injection-locked oscillator can be treated as a BPF. To perform a divided-by-2 operation in an injection-locked oscillator, the division ratio (*M*) must be 2 for an output signal. Based on the circuit topology of the proposed ILFD, two characteristics in the model should be adjusted for the proper locking range and the output power performance. First, the nonlinearity of the injector can be removed from the nonlinear mixer because the signal mixing operation is only generated in the transistors M_1 and M_2. In addition, the injected signal here is a differential signal, so that the injected signal, I_{RF}, should contain two signals with a phase difference of 180°, that is, $I_{RF}=I_{INJ}[\cos(2\omega t)+\cos(2\omega t+180°)]$. By satisfying the Barkhausen criteria, the locking range based on the derived formula

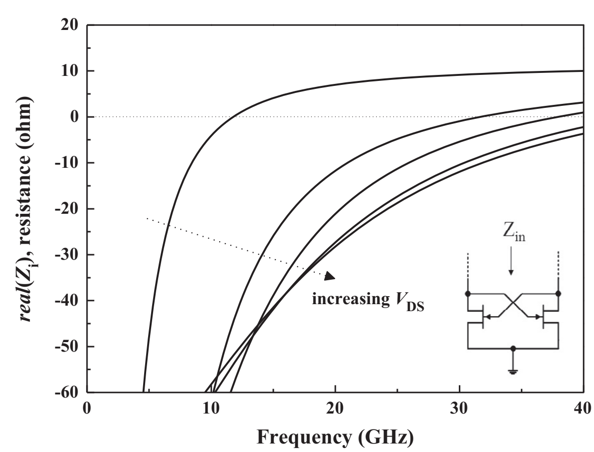

Fig. 3. Real-part impedance performances of the cross-coupled circuit depending on V_{DS}. (V_{DS}=0.2 V~1 V, step 0.2 V).

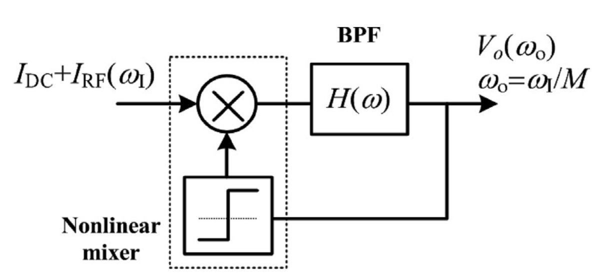

Fig. 4. Nonlinear feedback model for the injection-locked frequency divider.