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A reliable demodulator and a power regulation circuit with an accurate and small-size voltage reference in UHF RFID

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ABSTRACT

Key blocks used for Ultra High Frequency (UHF) Radio Frequency Identification (RFID) are designed in this paper, including a power regulation circuit and an ASK demodulator. The power regulation circuit is composed of a current mode voltage reference and a voltage regulator. The proposed current mode voltage reference is featured by the merits of small-size and high-accuracy. By optimizing the feedback factor of the voltage regulator, the chip size of the voltage reference is further reduced. The system design ensures the ASK demodulator has good performance in rejecting distortion and error-demodulation. Moreover, the threshold voltage compensation technology greatly improves the sensitivity of the demodulator. The proposed circuits have been fabricated under a SMIC 0.18 μm 2P4M EEPROM process. The power consumption of the voltage reference is 0.83 μW, the minimum operating voltage is 0.85 V, and the active area is 0.028 mm^2. The chip size of the ASK demodulator is 0.0078 mm^2. All of the proposed circuits were verified in a full UHF RFID chip, and tested through a commercial reader. Under a wireless circumstance, the power regulation circuit provides a stable 1 V power supply for the chip. The ASK demodulator correctly translates a full set of inventory command sent by the reader. According to the demodulated command, the tag chip feeds back the required data to reader.

1. Introduction

RFID has experienced a rapid development in various applications in recent years. Especially, the passive UHF RFID adopting ISO18000-6C EPC1-GEN2 standard is attracting a great deal of attention with a promising future. The applications can be found in supply chain, air and train package, intelligent transportation and asset-management system [1–3]. The passive UHF RFID tag chip features by low cost and long communication range. Low-cost calls for passive devices with the lowest possible count on the chip, and long communication range calls for ultra-low power consumption [2,3]. Both the requirements pose great challenges on the design of UHF RFID tag chip.

The architecture of the passive UHF RFID tag chip is shown in Fig. 1. It is composed of a RF/analog front-end, a digital core, and an EEPROM [3,4]. The main functions of the RF/analog front-end are power supply generation, power regulation, data demodulation and data modulation. In this paper, emphases are put on power regulation and data demodulation. The function of power regulation is realized by a power regulation circuit. The function of data demodulation is realized by an ASK demodulator:

1) Power regulation circuit: as shown in Fig. 1, the power supply voltage of passive UHF RFID V_{rect} is generated from the received RF signal through the voltage rectifier. However, V_{rect} which ranges from 1 V to 3 V shows a strong dependence on the power consumption of the tag chip and the distance between the reader and the tag. Furthermore, as the amplitude modulation affects the carrier, a significant ripple exceeding 500 mV occurs, as shown in Fig. 1. Providing a "clean" regulated power supply to the digital core and EEPROM is important to reduce gate overhead and power consumption [2]. Thus, a reliable, small-size power regulation circuit is crucial for the performance of UHF RFID. The power regulation circuit is composed of a voltage reference and a voltage regulator, as shown in Fig. 1, where the voltage reference provides a stable reference voltage V_{ref} for the voltage regulator. However, the voltage reference solutions dedicated for UHF RFID are rarely reported. In this paper, a new low-power current mode voltage reference is proposed to achieve the goals of small-size and high-precision simultaneously. Moreover, the feedback factor of the voltage regulator is set to be 2/3 to further reduce the chip size of the voltage reference. The proposed power regulation circuit provides a clean and stable 1 V power supply voltage named VDD for the tag chip.
2) ASK demodulator: the command and data are transmitted from UHF RFID reader to the tag chip using ASK modulation

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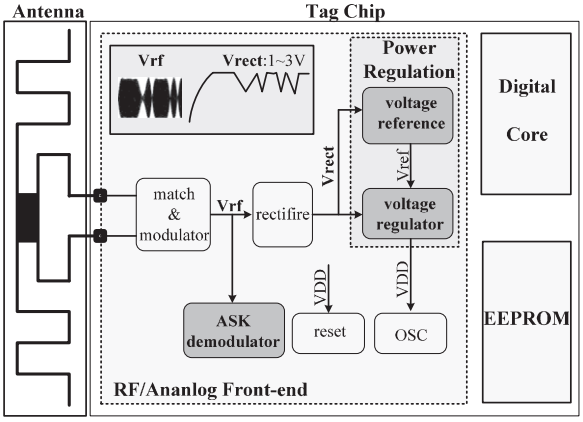

Fig. 1. Architecture of RFID chip with emphasize on the proposed circuits.

with a modulation depth ranging from 80% to100%. A reliable, low-power ASK demodulator with a small chip size is the key block to extract useful information from the high frequency carrier. In this paper, an ASK demodulator without big size passive devices is also proposed, with an active area of 0.0078 mm^2. Moreover, owing to the system design and the threshold voltage compensation technology, the demodulator has much less distortion and higher sensitivity than traditional demodulator.

This paper is organized as follows: Section 2 describes the realization of the power regulation circuit, including the voltage reference and the voltage regulator. The simulation results are also presented. Section 3 outlines detailed implementation of the ASK demodulator, plus the simulation results. Measurement results of the proposed circuits and the full RFID tag chip are presented in Section 4, followed by the conclusion in Section 5.

2. Power regulation circuit design

2.1. Voltage reference

The voltage reference used for UHF RFID tag chip should have a low power consumption and a small chip size. Moreover, restricted by cost and power, trimming is unacceptable for UHF RFID. Thus, it should have high accuracy. Traditional low-power, low-voltage reference can be classified into two types: one is based on the Banba solution with high accuracy [5–7]; the other one is the sub-threshold solution with low-power and small chip size [8,9]. The Banba solution utilizes the I–V curvature of pure PNPs (or NPNs) to generate zero temperature coefficient (TC) reference voltage V_{ref}, as shown in Fig. 2. However, it requires at least three big size PNP (or NPN) devices. Moreover, to achieve the goal of low power, three high resistance resistors (R1–R3) are required, which is stringent for the chip size. What is worse, the current consumption of Banba solution is always bigger than 2 μA [5–7]; The sub-threshold solution of Gianluca [8] utilizes the I–V curvature of MOSFETs biased in sub-threshold region to generate V_{ref}, as shown in Fig. 3. However, V_{ref} is directly related to the threshold voltage (V_{th}) of M1. For some processes, the variation of V_{th} is as big as 200 mV, so the variation of V_{ref} is also as big as 200 mV [1,8,9]. As a result, both the solutions cannot achieve the goals of high-accuracy and area-efficient at the same time.

In this paper, a low power voltage reference solution is proposed. To reduce the power supply voltage, current mode methodology is adopted. Besides low power, the proposed voltage

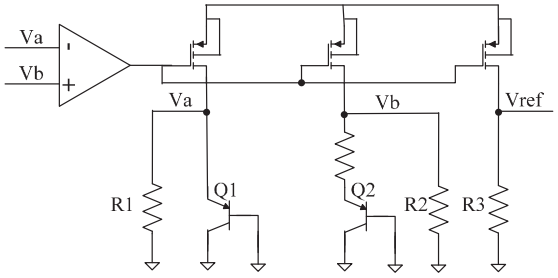

Fig. 2. Schematic of Banba solution.

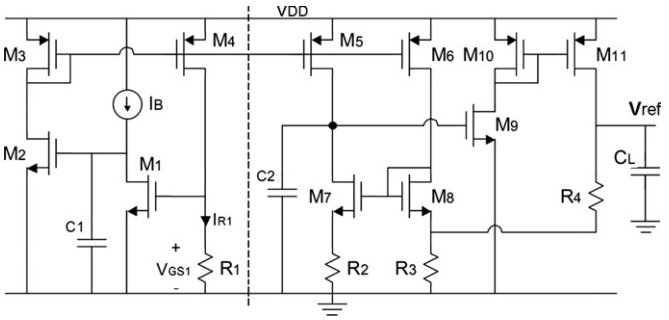

Fig. 3. Schematic of sub-threshold solution.

reference has the high precision merit of the Banba solution and the area-efficient merit of sub-threshold solution. Fig. 4 shows the schematic of the current mode voltage reference proposed in this design. V_{ref} is converted from the sum of the current proportional to absolute temperature (I_{PTAT}) and the current complementary to absolute temperature (I_{CTAT}). It is composed of a I_{PTAT} circuit, a I_{CTAT} circuit, a summing circuit and a startup circuit.

2.1.1. I_{PTAT} circuit

Traditional I_{PTAT} solution is based on the fact that the collector current I_c is exponentially increasing with V_{BE} of PNP device. I_{PTAT} is generated through the base and emitter voltage difference ΔV_{BE} of different PNP devices. However, this solution is discarded for its large chip size and high power consumption.

$$I_{DS} = S\gamma \exp\left(\frac{V_{gs}-V_{th}}{nV_T}\right)\left(1-\exp\frac{-V_{ds}}{V_T}\right) \quad (1)$$

where I_{ds} is the drain and source current, S is the ratio between the width and length of MOSFET, V_{ds} is the drain and source voltage difference of MOSFET, and V_{gs} is the gate and source voltage difference. $V_T = kT/q$, and it equals to 26 mV at room temperature, and γ is a ratio coefficient. n is a parameter defined as the differential of the gate voltage V_G to the cut off voltage V_p, and it ranges from 1 to 2.

When $V_{ds} > 4V_T$, the last term of I_{ds} can be neglected, then:

$$I_{DS} = S\gamma \exp\left(\frac{V_{gs}-V_{th}}{nV_T}\right) \quad (2)$$

As a result, I_{ds} and V_{gs} also show the same exponential correlation. Thus, I_{PTAT} can also be produced by the gate and source voltage difference ΔV_{GS} of two different MOSFETs.

The I_{PTAT} circuit is shown in Fig. 4, where M1, M2 and R1 are the core devices to generate I_{PTAT}. To save power, M1 and M2 are biased in sub-threshold region. Transistor M3 and M4 form current mirrors, hence $I_{DS3}/I_{DS4} = S_3/S_4$. The amplifier is added to form a feedback loop to guarantee a good power supply rejection ratio (PSRR).