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A 10 GHz wideband VCO with low KVCO variation

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ABSTRACT

This paper presents a novel topology for a 10 GHz voltage controlled oscillator (VCO). The design uses a differential delay cell architecture with four stages. It achieves a wide frequency range of (2–10) GHz and a maximum KVCO variation of 2.5 by using a voltage controlled resistor (VCR) that has a programmable size to reduce the impact of temperature and process corners variations. The design uses a 1 V supply and consumes a maximum power of 18 mW. It was extracted and simulated in 90 nm CMOS technology.

1. Introduction

Phase locked loops (PLLs) are used in most state of the art systems such as communication devices and microprocessors, where the requirement for high performance is critical. Furthermore, voltage controlled oscillators are the core blocks of (PLL) circuits. In the last few years, significant research has been done on high speed ring oscillator and LC-based VCOs [1–3]. One critical challenge was to achieve a wide frequency tuning range while maintaining a low KVCO variation. These two important parameters are defined in Eqs. (1) and (2). In some topologies, presented in [4,5], the overall frequency tuning range was below 3.

In [6], however, the VCO achieved a frequency from 1 GHz to 10 GHz while its KVCO has changed from 1 GHz/V to 26 GHz/V. So, the VCO, in [6], had a frequency tuning range of 10, and KVCO variation of 26 as per Eqs. (1) and (2).

$$\text{frequency tuning range} = \frac{\text{maximum frequency}}{\text{minimum frequency}} \tag{1}$$

$$\text{KVCO variation} = \frac{\text{maximum KVCO}}{\text{minimum KVCO}} \tag{2}$$

The VCO gain, KVCO, has a large impact on the performance of PLLs [7–13]. Eq. (3) describes the transfer function of a second-order PLL. Eqs. (4) and (5) define the PLL's natural frequency and damping factor, respectively. Large variations in KVCO adversely impact the PLL's stability, as can be seen in Fig. 1.

$$\text{closed loop transfer function} = H(s) = \frac{N(2\xi\omega_n s+\omega_n{}^2)}{s^2+2\xi\omega_n s+\omega_n{}^2} \tag{3}$$

$$\text{natural frequency} = \omega_n = \sqrt{\frac{I_p K_{vco}}{2\pi NC}} \tag{4}$$

$$\text{damping factor} = \xi = \frac{\omega_n RC}{2} \tag{5}$$

In Fig. 1, a closed loop transfer function is plotted while keeping all variables constant except for the KVCO. As shown in Table 1, a large KVCO variation not only changes the natural frequency but also causes large peaking. This will cause unstable operation.

The proposed VCO was designed using a differential delay cell architecture, because delay cells achieve a wider range of frequencies. Furthermore, using four stages offers the added ability to produce four quadrature outputs, which are used in data and clock recovery. The proposed design achieves the wide tuning range while maintaining a low KVCO variation.

This paper is divided into the following sections. In Section 2, the operation of the delay cell design will be reviewed and the new circuit design techniques and theory will be presented. Section 3 will explain the operation of the proposed design and give an example of its operation. Sections 4 and 5 contain the simulation results and the conclusions including a comparison table with other published work.

2. Theory and circuit design

The voltage controlled oscillator in [6] was used as a starting point for this new topology. Fig. 2 shows the block diagram of the VCO, and Fig. 3 shows the schematic of each differential delay cell.

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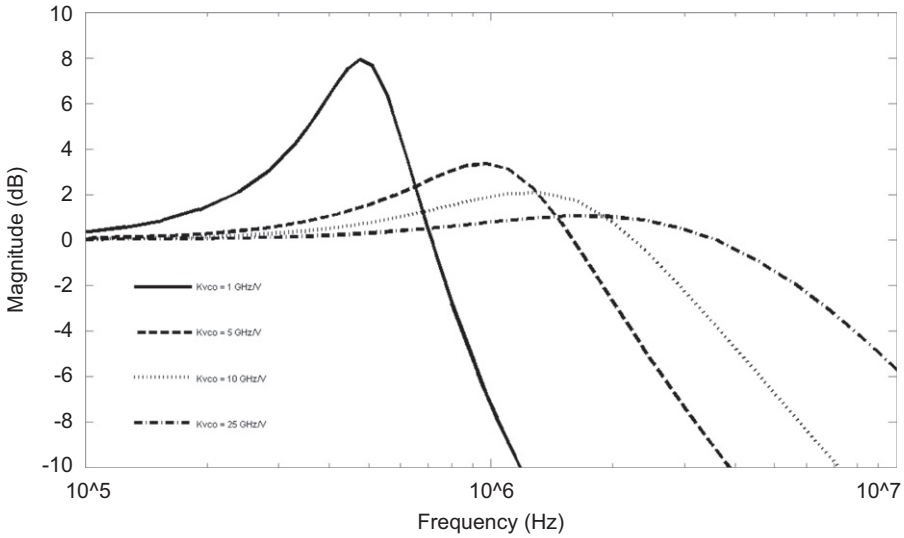

Fig. 1. Effect of KVCO on PLL transfer function (Table 1).

Table 1
Effect of KVCO variation on natural frequency, damping factor and peaking of PLL transfer function.

KVCO (GHz/V)	W_n (GHz)	ξ	Peaking (dB)
1	0.5	0.2236	7.9
5	1.125	0.5	3.5
10	1.59	0.7071	2.1
25	2.51	1.118	1

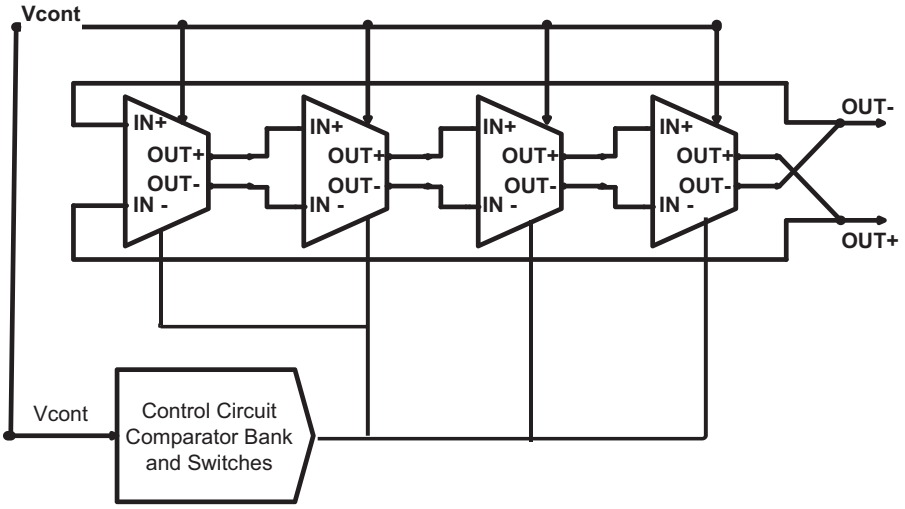

Fig. 2. Schematic of full VCO.

The modifications to [6] are the addition of the control circuit block and replacing each of the two voltage controlled resistors (VCRs) inside the delay cell by a programmable size transistor called MP variable (MPV). See Table 2 for details of transistor sizing.

This method is applied to the VCO in order to overcome the resistance changes due to process and temperature variations. It adds an extra mechanism of controlling the oscillation frequency rather than controlling it only by changing the control voltage, V_{cont}.

The operation of the initial delay cell is divided into two modes. For the time being, MPVa and MPVb are considered as regular non-programmable transistors.

- High frequency mode:
  This occurs at low control voltages. In this case, the larger size MPVa and MPVb transistors have low effective resistance because their source to gate voltage is large. The delay cell acts as a simple differential amplifier with active loading. In this mode, the voltage swing of the output nodes becomes smaller due to the increasing voltage drop across MN2. Also, the cross coupled transistors, MP1a and MP1b, are neglected due to their small current contribution and small drain to bulk capacitance compared to MPVa and MPVb.
- Low frequency mode:
  As the control voltage increases, the current contribution of