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Low-power area-efficient wide-range robust CMOS temperature sensors

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ABSTARCT

This paper proposes six different CMOS-based temperature sensor topologies by exploiting temperature dependence of MOSFET's threshold voltage V_T, the carrier's mobility μ and the resistivity of n-well resistors. The proposed temperature sensors are designed for a wide temperature range of -100 °C to $+120$ °C and exhibit resolutions in the range of 0.04–0.448 °C along with readout sensitivities in the range of 0.37–1.83 mV/°C. For accuracy enhancement, automated single-point calibration is implemented for all topologies in conjunction with an off-chip reference temperature sensor. These calibrated temperature sensors exhibit measured inaccuracies between 0.2 °C and 1 °C for the proposed temperature range. These temperature sensors are designed in 0.25 μm TSMC 1P/5M process and are embedded in a 5 mm × 5 mm imaging array readout IC to develop the thermal profile of the IC. The presented temperature sensors exhibit comparable performance metrics to state-of-the-art topologies in the literature with added advantage of a buffered output, which could be useful in case of a fast load drive and settling to implement faster control systems.

1. Introduction

Temperature sensing is a ubiquitous requirement of application domains extending from biomedical to industrial applications [1–3]. With advancements in integrated circuits technology, the trend of monolithic temperature sensing is increasing. Temperature sensors have evolved from bulky discrete sensors e.g. Bimetallic strips to area and power efficient on-chip junction and MOSFET sensors. Role of on-chip temperature sensors become even more important and critical when ICs have to operate at very high or very low temperatures when there is a need to develop insights about the distributed thermal profile of the silicon die. Wireless sensors are becoming popular especially for surface temperature measurements giving rise to further advancements in the design of temperature sensors. Market value for solid-state temperature sensors was valued at $539 million in 2011 and with an annual 5% growth rate, its market size is estimated to be $739 million by the year 2016 [4].

Historically, junction diodes and BJTs have been extensively used for temperature sensing due to their linear relationship and high readout sensitivity (2–3 mV/°C) with temperature albeit the fact that their linear operational temperature range is relatively limited [5–7]. BJT based temperature sensing generally rely on the CTAT or PTAT characteristics of forward bias junctions by measuring the base-emitter voltage or the difference in base-emitter voltages of two BJTs, respectively [8–11].

CMOS temperature sensors offer many advantages over their counterparts in terms of low-cost, small size and ease of use [12]. In a standard CMOS process, the temperature dependence of almost all the intrinsic devices such as resistors [13], MOS transistors [14], diodes [15,16] and bipolar transistors [17] can be exploited as temperature sensors. Majority of the approaches in the literature employ the BJT-like subthreshold region of MOSFETs by exploiting lateral and vertical BJTs inherent in a MOSFET [18–20]. Bandgap reference based approaches, which employ both CMOS and BJT, are abundant in literature, however, it is the BJT that is used as the temperature sensing device [21,22]. A well-known dynamic threshold MOS (DTMOS) based precision temperature sensor utilizes a PMOS, with its gate, drain and body terminals connected together, operating in subthreshold region [23]. The behavior of MOSFET under strong or moderate inversion has been relatively understudied and the available literature on the topic is scarce due to the preferred higher sensitivity offered by the subthreshold region.

MOSFETs in strong or moderate inversion can employ the temperature dependence of either threshold voltage or the carrier's mobility [24–26]. A simple but process-variation prone topology in [27] proposes a threshold-voltage dependent current-source for temperature sensing. The output current is followed by a current–frequency converter. A delay-line implemented by MOSFETs in linear region is proposed in [28] as a low power CMOS temperature sensor that uses the threshold-dependent turn-on delay as the temperature sensing parameter for the temperature range of 0–100 °C. Similarly, other topologies in [27,29–31] propose converting the temperature directly to or into period or frequency through its dependence on threshold voltage of the involved MOSFETs.

Along with sensitivity, another important parameter in CMOS-based temperature sensors is their accuracy over a large temperature range. Inaccuracies in temperature sensors can be

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compensated by on-chip and off-chip calibration. In case of BJTs, single-point calibration is enough to reduce the inaccuracy to ± 1 °C (3δ) [8]. In case of MOS-based temperature sensors, in some cases two-point calibration might be required due to different factor dominating the characteristic in different temperature ranges [2,32].

This paper presents a detailed theoretical framework to explain the temperature dependence of MOSFET threshold voltage and the carrier's mobility. Section 2 presents the design details of six different temperature sensors topologies designed in 0.25 μm TSMC 1P5M process. Section 3 presents the measurement results and compares the performance metrics of all the temperature sensors for a temperature range of -100 °C to $+120$ °C. Section 4 concludes the paper.

2. Theoretical framework

MOSFET based temperature sensors typically target the temperature dependence of either threshold voltage (V_{TH}) or the carrier's mobility (μ). Therefore, it is imperative to understand their behavior with temperature and to highlight different factors that dominate at different temperature ranges.

V_{TH} of a MOSFET can generally be defined as the voltage which initiates the inversion layer under the gate by attracting majority carriers from the source and drain regions. V_{TH}, for a PMOS, can be expressed as following:

$$V_{TH} = \phi_{MS} - \frac{Q_{ox}}{C_{ox}} - 2\phi_F - \frac{Q_{dep}}{C_{ox}} \tag{1}$$

$$V_{TH} = \phi_{MS} - \frac{Q_{ox}}{C_{ox}} - 2\phi_F - \gamma_p\sqrt{2\phi_F} \tag{2}$$

where ϕ_{MS} is the built-in work-function difference between polysilicon gate and the substrate. Q_{ox}/C_{ox} represents the voltage drop across the thin gate-oxide due to the trapped charge. ϕ_F represents the Fermi level of the substrate. Q_{dep} represents the immobile charge in the depletion region under the gate and while C_{ox} represents the gate oxide capacitance. γ_p represents body-effect coefficient. The first two terms in Eq. (1) and Eq. (2) above represent the potential difference to achieve a flat-band from the gate to the substrate, the third term represent the voltage required to make an equal electron and hole concentration in the channel beneath the gate and then the final term represents the voltage required to mirror the depletion charge under the gate. ϕ_F and ϕ_{MS} and their temperature dependence are typically formulated as following [33]:

$$\phi_F = \frac{kT}{q}\ln\left(\frac{N_B}{n_i}\right) \quad \phi_{MS} = -\frac{kT}{q}\ln\left(\frac{N_g}{N_B}\right) \quad n_i(T) = \sqrt{N_C N_V}e^{-E_g/2kT} \tag{3}$$

$$\frac{\partial(2\phi_F)}{\partial T} = \frac{1}{T}\left(2\phi_F - \frac{E_g}{q} - \frac{3kT}{q}\right) \tag{4}$$

where N_B and N_g represent the substrate and polysilicon doping level respectively, n_i represents the intrinsic carrier concentration and E_g represents the bandgap. N_C and N_V are the effective density-of-states for electrons and holes and k is Boltzmann's constant.

Eq. (5) gives the derivative of Eq. (2) with respect to temperature.

$$\frac{\partial V_{TH}}{\partial T} = \frac{\phi_{MS}}{T} - \frac{2\phi_F}{T} - \frac{\gamma_p}{\sqrt{2\phi_F}}\frac{\partial(2\phi_F)}{\partial T} + \frac{1}{T}\left(\frac{E_g}{q} + \frac{3kT}{q}\right) \tag{5}$$

Eq. (3) and Eq. (4) are then substituted in Eq. (5) and terms are rearranged as constants and temperature-dependent, which gives rise to simplified Eqs. (6) and (7). It can be seen from Eq. (7) that the temperature coefficient of the threshold voltage V_{TH} is a weaker function of the temperature as it mostly comprises of constants and a negligible constant-dominated inverse square-root relation. Therefore, it can be concluded that the temperature coefficient of V_{TH} stays relatively constant from temperatures as low as 77 K (-196 °C) up to 400 K (127 °C) [34,35].

$$\frac{\partial V_{TH}}{\partial T} = \left(-\frac{k}{q}\ln\left(\frac{N_g}{N_B}\right) + \frac{3k}{q}\right) - \frac{\gamma_p}{\sqrt{2\phi_F}}\frac{1}{T}\left(2\phi_F - \frac{E_g}{q} - \frac{3kT}{q}\right) + \frac{1}{T}\left(\frac{E_g}{q} - 2\phi_F\right) \tag{6}$$

$$\frac{\partial V_{TH}}{\partial T} = A_0 + \frac{\gamma_p k(1-2A_1)}{\sqrt{2kTqC_1 + qE_g}} + A_2 \tag{7}$$

$$A_0 = \left(-\frac{k}{q}\ln\left(\frac{N_g}{N_B}\right) + \frac{3k}{q}\right)A_1 = \ln N_B - \ln\sqrt{N_C N_V} A_2 = -\frac{k}{q}A_1 \tag{8}$$

The carrier mobility represents the ease with which carriers move in the semiconductor crystal and is given by $\mu = q\tau/m$ where m is the carrier effective mass and τ is the mean free time between the collisions which depends upon different scattering mechanisms [36]. The channel mobility can be expressed using Matthiessen's rule as shown in Eq. (9), where μ_{eff} and E_{eff} are the effective carrier mobility and electric field between source and drain regions, respectively. μ_{ph}, μ_{sr} and μ_{cb} are mobilities limited by phonon scattering, surface scattering and columbic scattering, respectively.

$$\frac{1}{\mu_{eff}(T,E_{eff})} \alpha \frac{1}{\mu_{ph}(T,E_{eff})} + \frac{1}{\mu_{sr}(T,E_{eff})} + \frac{1}{\mu_{cb}(T,E_{eff})} \tag{9}$$

Phonon scattering is due to collisions of carriers with lattice and is directly related to the periodic lattice vibrations and therefore to the absolute temperature. The interface roughness between the crystal silicon and the gate oxide gives rise to surface scattering of mobile charge carriers, depending upon the transversal electrical field created by V_{BS}. The columbic scattering is due to the charged centers near the Si–SiO interface, which repel the same charge carriers [37].

The surface scattering generally depends on electric field due to V_{BS} and is considered a weak function of temperature. The columbic scattering is generally described as having no temperature dependence, however, for ultra-low temperature (such as below 50 K) where the carriers have reduced thermal velocity, columbic scattering defines the effective mobility. For the temperature range of 100–400 K, phonon scattering dominantly defines the effective mobility of the carriers [38]. Therefore, Eq. (9) above can be assumed to have a constant and negative temperature coefficient in the above-mentioned temperature range. For instance, the electrons mobility at 100 K (2050 cm^2/Vs) and at 400 K (450 cm^2/Vs) can be roughly interpolated by a straight line [38].

3. Design details of the temperature sensors

3.1. Topology I: Source follower biased in strong inversion

Fig. 1 shows the common-drain source-follower stage with grounded-gate ($M1$ in strong-inversion), biased at constant current I_{BIAS} by M_2 while M_3 is the diode-connected current-mirror for M_2.

The expression for output voltage V_{OUT} is given by Eq. (10), which has both V_{TH} and μ as temperature sensitive parameters. $V_{OUT\text{-}SAT}$ has a pre-dominantly negative temperature coefficient due to threshold voltage. If M_1 is a short channel device, carriers can be pushed towards velocity saturation with an adequate V_{SD} across M_1, making μ insensitive to temperature, leaving V_{TH,M_1} as the only temperature sensitive parameter in Eq. (10). The threshold voltage of short-channel devices is prone to second-order