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Design of low phase noise and low power modified current-reused VCOs for 10 GHz applications

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ABSTRACT

In this paper, we present low phase noise and low power of the modified current-reused VCOs for 10 GHz application. Three chips are implemented by the standard 0.18 μm CMOS process. The improvement of the VCOs' three chips is described step by step.

The traditional current-reused circuit with a wide tuning range of 17.2% is presented in the first chip. It has a phase noise-118 dBc/Hz at 1 MHz offset and 5 mW core power dissipation with a voltage supply under 1.5 V. The performance of FOM is as high as −191.8 dBc/Hz. Extra NMOS cross-coupled pairs inside the traditional current-reused circuit in the second chip is proposed to speed up the oscillation and stability. The phase noise is −106.19 dBc/Hz and the core power dissipation is 3 mW with a voltage supply under 1.5 V. For the third chip, two dc level shifters are adopted to improve the symmetry of the output signal and to decrease noise interference. The phase noise and core power are -106.9 dBc/Hz and 2.88 mW, respectively. It also has a high performance of FOM with −182.4 dBc/Hz.

1. Introduction

During the past decade, the market for wireless communications requiring small, cheap, wide band, low phase noise and low power RF circuits has grown fast [1]. Voltage-controlled oscillators (VCOs) are one of the most important building blocks in these communications systems [2]. The major challenge lies in the design of fully integrated low phase noise and low power of voltage controlled oscillators (VCOs) that simultaneously have a wide tuning range.

Based on the literature, the circuit structure of the current-reused oscillator has lower power consumption compared to that of the conventional LC-VCO [2,3]. At high operation frequency, the oscillator usually needs large bias current to provide enough transconductance (g_m) [2]. In this work, the proposed current-reused VCOs, both with traditional current-reused and without a NMOS cross-coupled pair, and with NMOS cross-coupled pair topologies are discussed.

The paper is organized as follows. In Section 2, the design of a low power current reused VCO circuit with NMOS cross-coupled pair topology is proposed. We fixed the supply voltage and set the same active device transconductance. Next, we compare the performance between chip1 and chip2. We also added a dc level shifter in the circuit to improve the symmetrical output signal and phase noise with description by chip3. In Section 3, the measured results of the proposed VCO are addressed. The comparisons of the circuit performance are also described. Finally, the conclusions are in Section 4.

2. Circuit design

The presented topologies in this paper are based on a current-reused LC oscillator [3]. The schematic diagrams of the proposed VCOs are shown in Fig. 1(a) shows chip1, that is the traditional current-reused circuit. Fig. 1(b) is chip2, which is the proposed circuit with additional an NMOS cross-coupled pair in the interior of the Fig.1(a). When the NMOS cross-coupled pair is added in the circuit, it provides extra negative resistance to compensate for the passive element loss of the LC tank and improved oscillator stability.

In the beginning, we will explain the reason why we considered the current-reused VCO topology is used for low power design. The traditional cross-coupled pair was chosen to be compared with current-reused topology, and we discuss the differences between them. In the view of power consumption, if the drawing current can be reduced, then the power can also be decreased when the supply voltage of the circuit is fixed.

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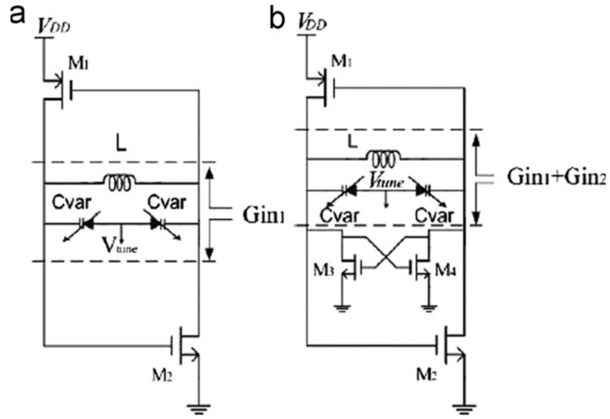

Fig. 1. Schematic diagrams of the two VCOs, (a) traditional current-reused circuit (chip1), (b) proposed negative resistance enhancement current-reused circuit (chip2).

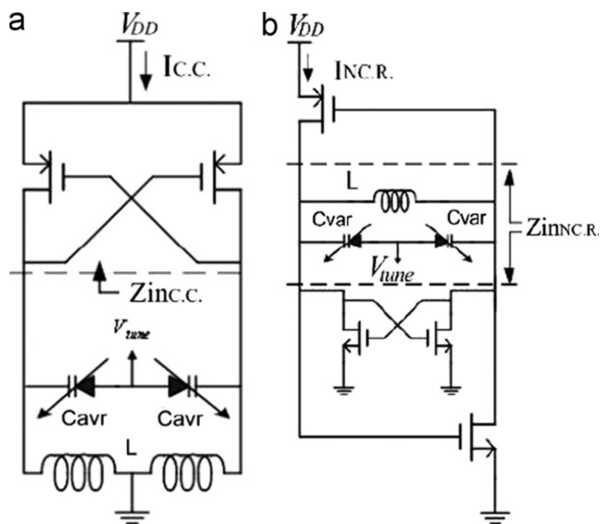

Fig. 2. Schematic diagrams of VCOs, (a) Cross-coupled VCO, (b) Proposed current-reused VCO.

Therefore, we set the same active device transconductance to investigate the differences between traditional cross-couple pairs and the current-reused circuit in Figs. 2 and 3.

First, we set the same transconductance between the cross-coupled VCO and the current-reused VCO in Fig. 3(a) under the same supply voltage VDD. In the second step, we saw that the proposed current reused topology draws 1.48 mA and the cross-coupled pairs topology draws 16.9 mA. We found that the available current of the current-reused circuit is extemporarily smaller than the in cross-coupled pairs. The results of drawing current in Fig. 3(b) shows that the proposed current-reused topology needs less power than that of the cross-coupled pairs topology for starting up oscillation. This result is very interesting and attractive for engineers planning to design low power applications.

2.1. Current-reused topology with additional NMOS cross-coupled pair

In Fig. 4, we can analyze several important parts of this simple LC tank VCO structure [4]:

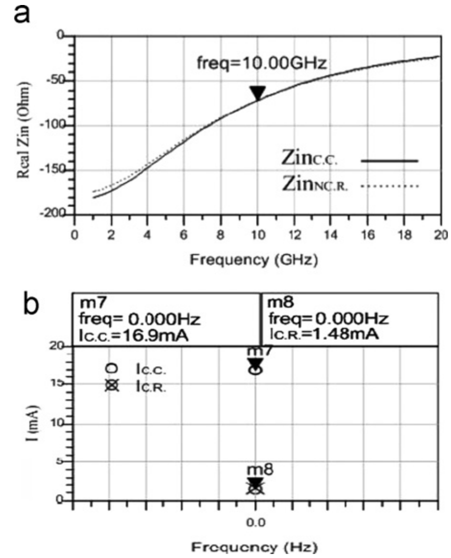

Fig. 3. Properties between traditional cross-couple pairs (C.C.)and negative resister enhancement current-reused circuit(NC.R.), (a)negative resistance value (ZinC.C. and Zin.NC.R.) of circuits, (b) current-consumption of circuits (IC.C. and INC.R.).

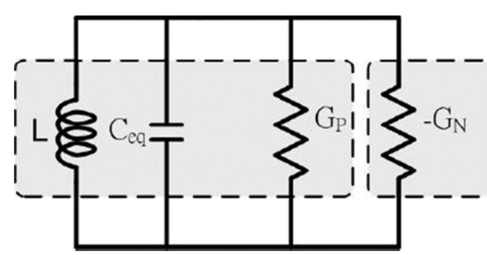

Fig. 4. Simple LC tank VCO structure.

2.1.1. The part A—passive LC tank

The tank circuit consists of an inductor with high Q value ($Q=14$) and varactor components. The model values for the inductor and varactor are selected to control oscillatory frequency. Where, G_P denotes the passive element loss of LC tank.

2.1.2. The part B—active circuit

An active circuit is used to provide negative resistance ($-G_N$) and compensate for the loss of the LC tank.

In Fig.1(a), we can obtain the input conductance G_{in1} with the following equation [5]:

$$G_{in1} = -\left(1/gmp_1 + 1/gmp_2{}^{-1}\right) \quad (1)$$

If G_p denotes the passive element loss of the LC tank, then the start-up condition for oscillation is the following:

$$G_p + G_{in1} \leq 0 \quad (2)$$

The proposed current-reused VCO is with an additional NMOS cross-coupled pair, and if the transistors sizes of M3 and M4 are the same, the input conductance G_{in2} can be reduced as follows:

$$G_{in2} = -gmn_3/2 \quad (3)$$

Eq. (2) becomes the following equation:

$$G_p + (G_{in1} + G_{in2}) \leq 0 \quad (4)$$