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A low-area full-division-range programmable frequency divider with a 50% duty-cycle output

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ABSTRACT

This work presents a full-division-range programmable frequency divider with 50% duty-cycle output. The proposed programmable frequency divider includes a programmable counter (PC) and duty-cycle-improved circuit (DCIC) to achieve full-division-range, low-area, and close-to-50% duty-cycle output from an input clock with an arbitrary duty cycle. A chip was fabricated using 0.18-μm standard CMOS process with a 1.8-V power supply. The experimental results show that the proposed programmable frequency divider can operate correctly when input clock frequency ranges from 1 MHz to 1 GHz and division ratio ranges from 1 to 63. For an input divisor of 20 with input clock frequencies of 700 and 1 MHz and duty cycles of 20% and 99.5%, the output duty cycles were 50.4% and 50%, respectively. The total power consumption of the proposed programmable frequency divider was only 0.62 mW at 700 MHz, and the active die area was only 0.125×0.05 mm^2.

1. Introduction

In the last decade, most conventional frequency dividers were used in phase-locked loops (PLLs) to generate a high-frequency output clock from a stable low-frequency external signal [1,2]. However, because of the increased system complexity and clock variants in recent years, a programmable frequency divider is crucial for various applications [3]. These applications can generally be identified by their requirement for 50% duty-cycle input clocks, such as (1) switched capacitor-based circuits (SCC), for example, in the pipelined analog-to-digital converter (ADC), a clock with 50% duty cycle ensures that each stage of the pipelined ADC has the same magnitude of time to settle [4]; (2) DRAM, which doubles the data transfer rate using rising and falling edge of 50% duty-cycle clock input [5]; (3) low-power (LP) systems, in which the dynamic frequency scaling (DFS) technique is used to achieve the so-called low-power consumption mode by altering the operating frequency using a programmable frequency divider [6]; and (4) other circuits, in which various 50% duty-cycle input frequencies are used in various circuits by altering the division of the divider [7], as shown in Fig. 1. These applications require an accurate 50% duty-cycle input clock and variable operating frequencies for optimal performance. Therefore, a wide division ratio and low-area programmable frequency divider with 50% duty-cycle output are useful for these applications. Although previously reported programmable frequency dividers [1,2,8,9] can provide wide division ratios, they do not produce 50% duty-cycle output clocks, which limit the potential applications. Additionally, the narrow pulse width is sensitive to process, voltage, temperature, and loading (PVTL) variations, resulting in incorrect operations and reduced system robustness. This disadvantage can be avoided by connecting a divide-by-two circuit after conventional programmable frequency dividers, regardless of the input duty cycle. However, such an approach limits the divisor ratio of these programmable frequency dividers, which narrows the applicable area. Therefore, several programmable frequency dividers [3,10] have been reported to improve the output duty cycle without connecting a divide-by-two circuit. Although a wide range of input divisors is available for these programmable frequency dividers, they cannot achieve full-range division.

This work presents a programmable frequency divider that can achieve a full-range division and improve the output duty cycle to 50%. The proposed programmable frequency divider has four crucial advantages: (1) the reload generator and duty reload generator are simple and can be easily extended for higher division ranges; (2) a continuous and full-range divisor can be achieved from 1 to 2^{n-1}; (3) the duty-cycle output pulse width is approximately 50% and varies by less than 0.7% for various input divisors when the input duty cycle ranges from 40% to 60%; and (4) the core area is small.

The remaining part of this work is organized as follows: Section 2 presents a brief description of the architecture of conventional frequency dividers; Section 3 introduces the proposed programmable

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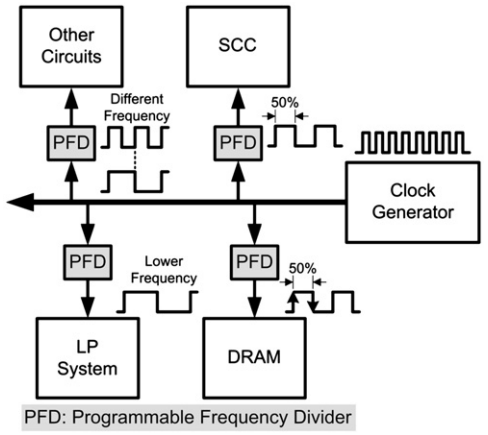

Fig. 1. Applications of the programmable frequency divider with an improved duty-cycle output.

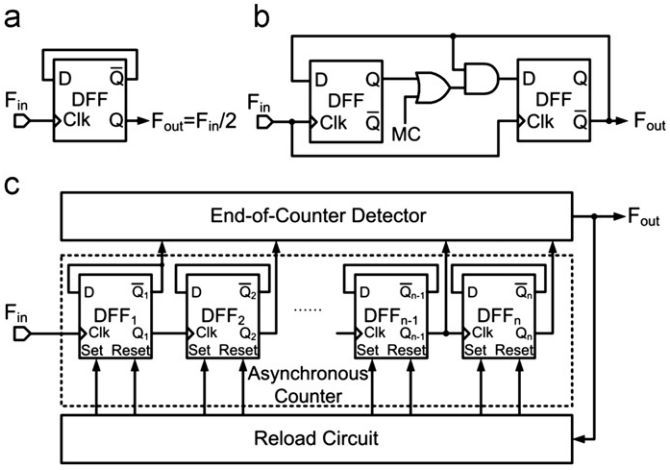

Fig. 2. Types of frequency dividers. (a) Divide by 2, (b) Divide by 2/3 and (c) Programmable.

frequency divider design; Section 4 provides the experimental results; and lastly, Section 5 offers a conclusion.

2. Conventional frequency dividers

Generally, three types of frequency dividers are used. The most simplified architecture is the divide-by-two circuit [9], as shown in Fig. 2(a). This circuit features a low-power and low-area design, and 50% duty-cycle output because it divides the input frequency by two uniformly. However, this type of architecture fixes the division ratio range to 2^n, thereby preventing the achievement of a continuous and full-range division. To extend the division range of a divide-by-two circuit, previously studies proposed the dual modular divider [9,11–13], as shown in Fig. 2(b). The feature of this circuit is that it includes a divisor-controlled signal MC. When the signal MC is high, the dual modular divider serves as a divide-by-two circuit. Conversely, when the signal MC is low, the output of the OR gate is no longer maintained at a high logic level, which alters the divisor into three. Although the area of a dual modular divider is slightly larger than that of a divide-by-two circuit, it includes divisor options; thus, it is called a dual modular divider. However, because the circuit is dual modular, it does not provide 50% duty-cycle output, which cannot be compensated for by resizing the transistors. Thus, although dual modular dividers provide a choice of divisors, they are insufficient for applications that require a wide division ratio. Therefore, previous studies have presented a wide-division-ratio divider [9,14,15]. The wide-division-ratio programmable frequency divider combines the D flip-flop of divide-by-two circuit with the divisor-controlled signal of dual modular divider to achieve a wide division ratio of $2–2^{n-1}$, as shown in Fig. 2(c). However, the output duty cycle is considerably narrow because the output clock F_{out} is high only when the reload circuit reloads the asynchronous counter. Furthermore, in addition to cascading D flip-flops, a reload circuit and an EOC detector are also added, thereby increasing the area and costs, which limit use for applications.

To overcome these disadvantages, this study proposes a new full-division-range programmable frequency divider with 50% duty-cycle output. The proposed architecture retains the asynchronous counter to maintain a full-ratio division, provides a low-area feature, and can be easily extended to higher divisor ranges by merging the reload circuit and EOC detector. Moreover, the proposed programmable frequency divider uses a low-area duty-cycle-improved circuit (DCIC) to improve the narrow output duty cycle of conventional programmable frequency dividers to 50%. Furthermore, the input clock can be arbitrary duty-cycle signals.

3. Proposed programmable frequency divider

3.1. Proposed architecture and operation principle

Fig. 3 shows the proposed programmable frequency divider, which comprises a programmable counter (PC) and DCIC. Signal F_{in} is the input clock and signal IN[1:n] is the input binary divisor. Internal signal $Q[1:n-1]$ is the binary counting result from the PC, and signal Reload is the output of the PC. Additionally, the signal reloads the full divider. Signal F_{out} is the output clock of the programmable frequency divider. To clarify the operation principle, Fig. 4 shows a timing diagram of the programmable frequency divider when input divisor is 6. When the input clock F_{in} is activated, the PC begins counting and simultaneously sends the resulting signal $Q[1:n-1]$ to the DCIC. When the PC counts down to the complement of input divisor IN[1:n], it generates a reload signal to reload the programmable frequency divider. The signal Reload is also sent to the DCIC to charge the output clock F_{out} to high. Then, because reloading is already accomplished, the PC discharges the signal Reload to low. Subsequently, the DCIC generates an internal signal Duty Reload to discharge output clock F_{out} to low as the PC counts down to suitable results. Here, the complement output $\overline{F_{out}}$ is charged to high, which discharges the signal Duty Reload to low using the DCIC. Finally, a period of output is generated, providing an output frequency that is one-sixth of the input clock frequency and 50% of the output duty cycle.

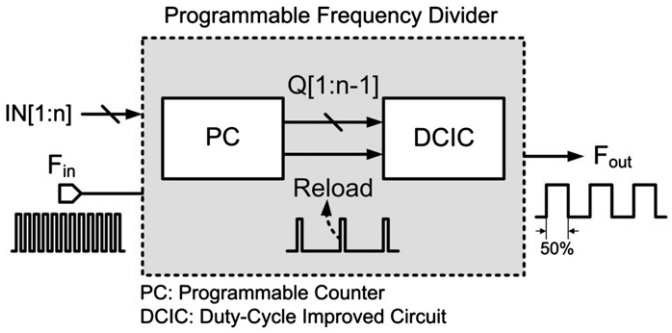

Fig. 3. Proposed programmable frequency divider.