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A 1-V, 1.2-mA fully integrated SoC for digital hearing aids

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ABSTRACT

Both power and size are very important design issues for hearing aids. This paper proposes a fully integrated low-power SoC for today's digital hearing aids. The SoC integrates all the audio processing elements on single chip, including the analog front-end, digital signal processing (DSP) platform and class-D amplifier. Also, the low-dropout voltage regulators and internal clock generator are both integrated to minimize the system overall size. The 24-bit DSP platform comprises an application-specific instruction-set processor and several dedicated accelerators to achieve a trade-off between flexibility and power efficiency. Three critical hearing-aid algorithms (wide dynamic range compression, noise reduction and feedback cancellation) are performed by the low-power accelerators. The proposed SoC has been fabricated in SMIC 130 nm CMOS technology. The measurement results show that the analog front-end has up to 88 dB signal-to-noise ratio. And the DSP platform consumes about 0.86 mA current at 8 MHz clock frequency when executing the three algorithms. The total current consumption of SoC is only 1.2 mA at 1 V supply. In addition, the acoustic test results indicate that the SoC is one promising candidate for hearing-aid manufacturers.

1. Introduction

Designing the ICs for modern hearing aids poses many challenges and is a constant compromise between power, size and performance. Today, more and more features are added to the products. This poses a formidable challenge to the ICs designers, due to the very low supply voltage and limited power consumption budget. Most hearing aids are powered by zinc–air batteries, which supply the 1.1–1.4 V voltage and about 220 mA h capacity (for zinc–air A13). The current of ICs should be kept under 1.5 mA to support 12-day normal using with 12 h every day. Meanwhile, the size of hearing aids is constantly decreasing, making them invisible today. Thus, the size of ICs is critical for the final size of products. It is necessary to integrate all the components (analog, digital, power supply and clock) into a single chip and finally package the whole system together.

Previous works about hearing aids ICs focus on analog chain and digital hearing algorithm, respectively. The mix-signal IC [1] includes all analog processing elements, consuming 270 μA at 1.1 V. A dedicated digital circuit with programmable parameters is adopted to support basic auditory compensation function. The paper in [2] presents a low-power analog chip for hearing-aid. Signal processing is performed through an analog chain, with digital user trimmers. The programmable DHA SoC (System on a Chip) [3] also includes the whole analog chain and executes PREVA algorithm to obtain fast and accurate gain for hearing loss. The above works mainly focus on analog signal processing and do not meet the feature requirements of today's high-end hearing aids, such as feedback cancellation (FBC), noise reduction (NR) and wide dynamic range compression (WDRC) [4,5]. Other studies focus on hearing algorithms and adopt different hardware implementations. A dedicated processor is developed to meet the requirement on area and power consumption for a hearing-aid system, through a series of software/hardware optimizations [6]. The paper in [7] presents mandarin-specific hearing algorithms and implements them with dedicated hardware. Then, a much more flexible computing platform is proposed [8]. The platform composes four processing elements. Each one includes a RISC (Reduced Instruction Set Computer) and several hardwired accelerators.

This paper proposes a fully integrated SoC for the first time, which covers the critical features of today's hearing aids. The mixed-signal SoC integrates all the signal processing elements on single chip, including analog front-end (AFE), digital signal processing (DSP) platform and class-D amplifier. The voltage regulators and internal clock generator are also integrated to minimize the system overall size. Three major algorithms (WDRC, NR, and FBC) are performed on the power-efficient and flexible DSP platform. Measurement results indicate that the proposed SoC is one promising candidate for hearing-aid manufacturers.

The rest of this paper is organized as follows. Section 2 describes the overview of the SoC architecture. Section 3 shows three major hearing algorithms and describes the hardware organization of DSP

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platform in detail. In Section 4, the analog design considerations and analog chain including AFE and class-D amplifier are shown. The real chip implementation and measurement results are presented in Section 5. Finally, conclusions are drawn in Section 6.

2. System architecture

Fig. 1 shows the system block diagram for the proposed SoC and a typical hearing aids system. The audio AFE includes the programmable gain amplifier (PGA) and analog-to-digital converter (ADC). The PGA amplifies the microphone's output to achieve a higher signal-to-noise ratio (SNR). Also, the PGA attenuates the large input signal to avoid the overload to 1 V ADC. The 2nd-order 3-bit Sigma-Delta ADC outputs a 3-bit data at 2.048 MHz rate. The data are down-sampled by a factor of 128 through a decimation filter. Then, the 16-bit 16-KHz samples are processed on a power-efficiency DSP platform. The 24-bit DSP platform comprises an application-specific instruction-set processor (ASIP) and several dedicated accelerators. Three major algorithms (WDRC, NR, and FBC) are performed by the dedicated accelerators. The ASIP controls the signal processing flow and executes extended hearing-function at assembly level. The class-D amplifier is comprised of 4th-order Sigma-Delta modulator and an H-bridge driver. The modulator receives 16-bit 16-KHz audio data from DSP and converts it into a 64-times oversampled, 1-bit PDM (Pulse Density Modulated) data stream. The H-bridge converts the 1.024 MHz, 1 bit PDM data stream into a low-impedance, differential output voltage waveform, which drives the zero-biased receivers for hearing aids.

The SoC integrates multiple voltage regulators on chip. The AFE and DSP have their own power supplies to achieve exceptional audio quality. The low-dropout (LDO) voltage regulator for DSP has a programmable output voltage (0.75 to 1.1 V with 50 mV per step) that allows the selection of the lowest digital supply depending on different work cases. The charge pump generates 3.3 V voltage for all pads and external EEPROM memory, which stores parameters and assembly programs for DSP. Based on the fully integrated SoC, the hearing aids system is very compact. The system consists of zinc–air battery, microphone, receiver, SoC, EEPROM, and decoupling capacitors. If the later three components are packaged together in a system-in-package (SiP) approach, the final system size will be further reduced.

3. Algorithms and DSP platform

3.1. Algorithms for hearing aids

The primary goal of hearing aids is to improve the speech understanding for hearing impaired person. Three critical features are necessary for today's digital hearing aids, which are wide dynamic range compression, adaptive noise reduction and adaptive feedback cancellation [4,5]. The wide dynamic range compression applies different gains on different input sound levels to map the normal dynamic range into the perceptible range. The noise reduction removes the background noise to improve speech quality and intelligibility. Feedback cancellation suppresses the acoustic feedback oscillation caused by the sound leaking from loudspeaker to the microphone. Most of the hearing algorithms are subband based, which requires an analysis filterbank and a corresponding one for signal synthesis.

3.2. Digital signal processing (DSP) platform

For the algorithm implementation, power efficiency and flexibility are the main concern for DSP hardware designers. The current budget for DSP platform is only about 500–900 μA. Meanwhile, platform should be flexible enough to meet the algorithm modification and personalized requirements. A novel DSP platform is proposed in this paper, which consists of an ASIP and dedicated accelerators, as shown in Fig. 2. The dedicated accelerators execute the fixed and intense computing task for hearing aids. There are five accelerators in current platform, which are weighted overlap-add analysis/synthesis (WOLA_A and WOLA_S) filter bank, NR, WDRC, and FBC accelerators. Each accelerator is implemented as ASIC version for power efficiency. The ASIP controls the signal processing flow by interrupt scheme. Other user-defined algorithms can be executed on ASIP at assembly level.

The DSP platform provides considerable flexibility at three different levels. Firstly, the ASIP supports the assembly-level programming. The ASIP is actually a 24-bit data width, 5-pipeline RISC core with optimized instruction-set. Secondly, each accelerator is reconfigurable with special function registers. For example, the FFT hardware in WOLA_A can be configured as 16, 32 or 64-point. Thirdly, though the dedicated accelerators are nonprogrammable, the carefully designed interconnection between the ASIP and

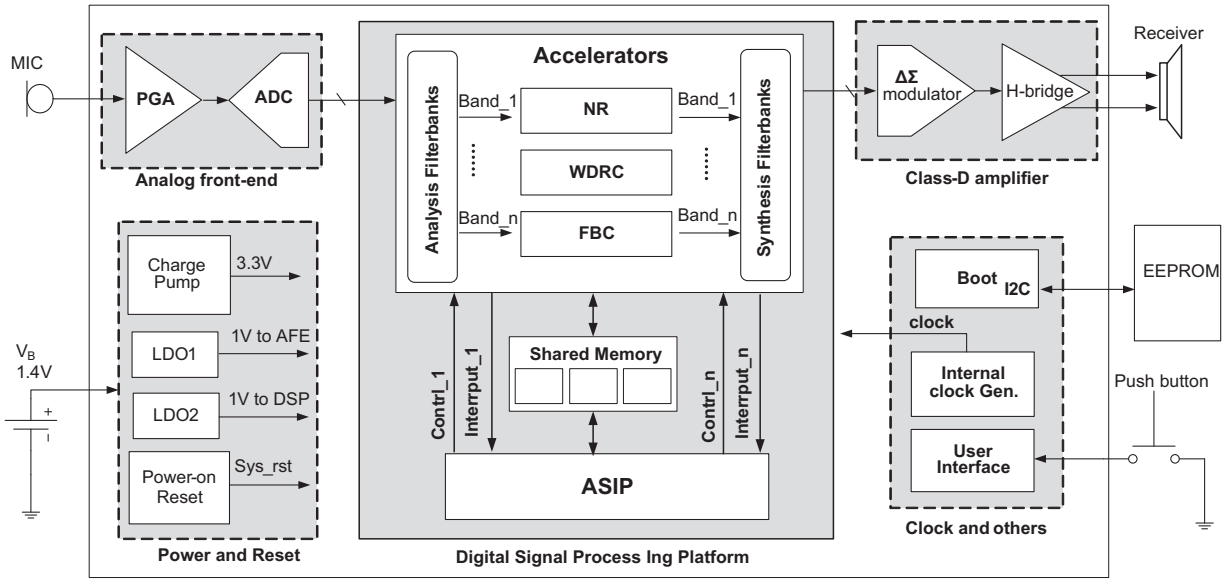

Fig. 1. System block diagram for the proposed SoC.

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