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A low-distortion multi-bit sigma–delta ADC with mismatch-shaping DACs for WLAN applications

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ABSTRACT

A low-distortion feed-forward MASH2$_{4b}$-2$_{4b}$ sigma–delta analog-to-digital converter (ADC) for wireless local area network (WLAN) applications was presented. The converter exhibits improved performances than the ADCs which have been presented to date by adding a feedback factor in the second stage and employing a 2nd-order noise-shaping dynamic element matching (DEM) scheme. The feedback factor induces a zero in the noise transfer function (NTF) and therefore improves the in-band signal to noise and distortion ratio (SNDR) of the modulator. The mismatch-shaping DEM was introduced and applied to the 4-bit DACs in this paper to improve the resolution and linearity of the ADC. Fabricated in a 0.18 μm CMOS process with single 1.8 V supply voltage, the converter achieves a peak SNDR of 85.4 dB over a 10 MHz bandwidth which implies an effective number of bits (ENOB) of 13.90-bit. The spurious free dynamic range (SFDR) is –94 dB for a 1.25 MHz@–6dBFS input signal at 160 MHz sampling frequency. The occupied area is 0.44 mm^2 and dissipation power 23.4 mW.

1. Introduction

Emerged in 1980s, the wireless local area network (WLAN) technologies serve as an extension to, or as an alternative for, a wired LAN by using radio as the transmission communication network operating over a limited medium [1–3]. By using wireless LAN, users can access shared information without having to look for a place to plug in [4–6]. However, to achieve higher data rates in emerging wireless generations such as IEEE 802.11b/g, the data converters in the processing chain of WLAN must be able to handle wider bandwidths at lower noise and distortions [7–9]. The requirements that the A/D converter has to fulfill are set by both the standard characteristics and the receiver architecture. Generally, together with the link budget of the receiver, such as zero-IF WLAN 802.11b receiver, the radio specifications of the WLAN lead to a dynamic range of about 60–80 dB for the ADC for a 10 MHz bandwidth.

The sigma–delta modulation technique has been widely used in the A/D and D/A converters [10–15], programmable PAs (Power Amplifiers) [16], fractional-N PLL (Phase Locked Loop) [17] and so on for several years. It employs noise shaping and oversampling techniques to move quantization noise or mismatching noise away from the interested band in order to remove them by filtering. Compared to other structures, the sigma–delta scheme makes low-power and low-cost while high resolution and SNDR achieved.

This paper presents a multi-bit sigma–delta A/D converter at a clock rate of 160 MHz. Data conversion is done in baseband for frequencies up to 10 MHz and therefore, it can be used in a WLAN receiver. In order to further improve the performance of the converter, some modifications and optimizations of conventional architectures were made in this paper. A feedback factor was added into the second stage to change the noise transfer function and thus improve the SNDR. The linearity of the modulator is directly related to the linearity of the DACs in the feedback path [18]. To minimize the mismatch effects which could greatly degenerate the linearity of the 4-bit DACs, 2nd-order sigma–delta DEM was employed to provide a much better mismatch attenuation.

2. Improved architecture

The sigma–delta modulator in this work basically corresponds to a MASH2$_{4b}$-2$_{4b}$ architecture which can achieve both higher SNDR and SFDR over a 10 MHz bandwidth. Employing of multi-bit quantization has the advantages of not only providing sufficiently low quantization noise level but also allowing a drastic reduction of the power consumption. Integrators are used to accumulate the difference between the input signal and the feedback signal, and since the feedback DAC signal can track the input signal precisely with multi-bit quantization, the amount of charge flowing through the integrators is reduced at each clock cycle [18].

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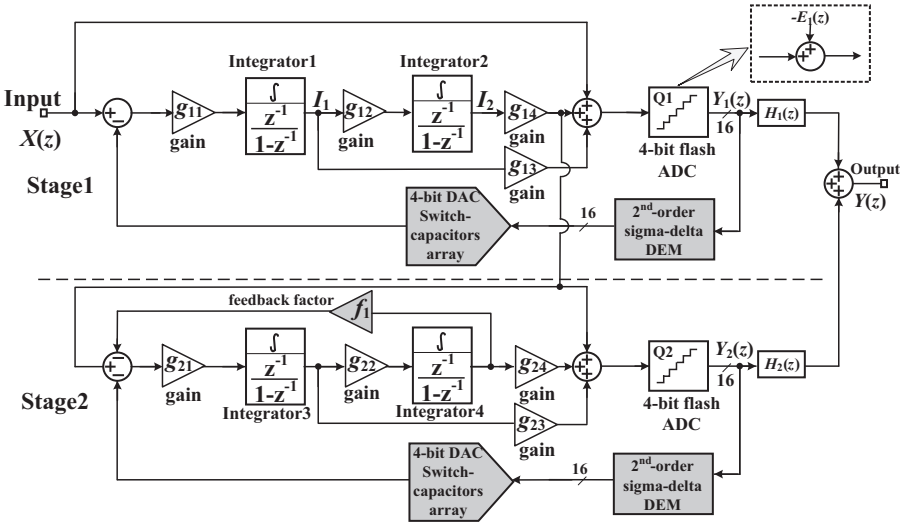

Fig. 1. The overall architecture of the MASH2$_{4b}$-2$_{4b}$ sigma–delta modulator.

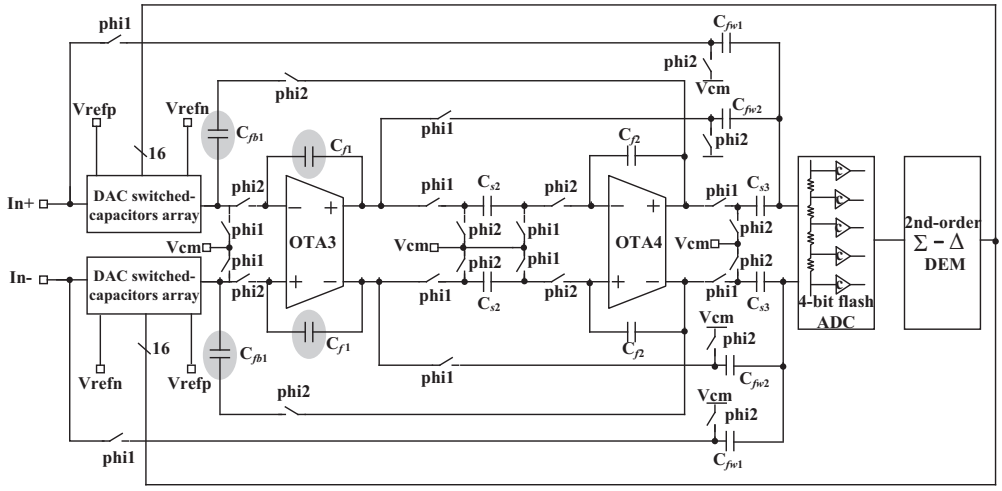

Fig. 2. Full differential switched-capacitor CMOS implementation of the second stage.

The theoretical SNDR of a sigma–delta modulator can be given by

$$\mathrm{SNDR} = \frac{3\pi}{2}\cdot\frac{2L+1}{\pi^{2L+1}}\cdot(2^B-1)^2\cdot \mathrm{OSR}^{2L+1} \tag{1}$$

where L is the order of the modulator, B the number of bits of the quantizer, and OSR the oversampling ratio which is defined as the ratio of the sampling frequency to the Nyquist frequency. For the WLAN application featured high data rates, OSR and L should not be made much higher considering of high sampling frequency, circuit complexity and power dissipation. In this design, an OSR of 8 and L of 4 were chosen as a trade-off between the sampling frequency and the 10 MHz bandwidth. To further improve the SNDR of the converter, 4-bit quantizers were employed in both stages. The overall architecture of the sigma–delta modulator is shown in Fig. 1.

The input signal is injected at the output of integrators so that the dc component proportional to the input signal can be canceled and therefore reduce the swing requirements. The linearity of the DACs in the feedback path is a critical issue. Conventionally, the 4-bit flash ADC converts the analog signal to a 16-bit thermometer code and then, feeds them directly into the DAC in which elements will be selected in a thermometric algorithm. Obviously, this scheme suffers from mismatches between elements due to non-idealities in practical fabrication and therefore large distortions appear in the output spectrum. In order to decrease the mismatch noise of the 4-bit DACs, 2nd-order mismatch-shaping DEM which spectrally shapes the mismatch noise to high frequency domain and thus attenuates the in-band noise is applied to the DACs.

Each stage is in fact a second-order, 4-bit feed-forward architecture and the second stage has nearly the same structure as the first one in the absence of the added local resonator feedback factor f_1. Assuming that the quantizer gain used in this modulator equals unity and the quantization noise $E_1(z)$ is simply additive and white, the outputs of the integrators1 and integrator2 in the first stage can be given respectively by

$$I_1(z) = \frac{g_{11}z^{-1}(1-z^{-1})}{1+(g_{11}g_{13}-2)z^{-1}+(1-g_{11}g_{13}+g_{11}g_{12}g_{14})z^{-2}}\cdot E_1(z) \tag{2}$$

and

$$I_2(z) = \frac{g_{11}g_{12}z^{-2}}{1+(g_{11}g_{13}-2)z^{-1}+(1-g_{11}g_{13}+g_{11}g_{12}g_{14})z^{-2}}\cdot E_1(z) \tag{3}$$

It can be observed from (2) and (3) that the integrators process just the quantization noise. As a result, the output swing of the integrators is reduced and the requirements of the operational amplifier can be relaxed greatly. This is the advantage of the feed-forward architecture. The output of the first stage $Y_1(z)$ can be