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Fast and energy-efficient low-voltage level shifters

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ABSTRACT

This paper presents two novel low-voltage level shifter designs: one based on cross-coupled PMOS transistors and the other using current mirror structure. These two level shifters are designed to address the problems of the existing state-of-the-art level shifters. Simulation at 65 nm shows that both of the proposed level shifters achieve significantly better performance (up to 12 ×) and energy consumption (up to 8 ×) than the state-of-the-art level shifters with similar or less area consumption while operating from near-threshold to super-threshold region, making them optimal for level shifting in low-power systems with multiple scalable voltage domains.

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1. Introduction

Voltage scaling has been demonstrated to be effective in reducing the energy consumption of digital and mixed-signal circuits [1,2]. It has been found that the minimal energy can be achieved when the supply voltage is lowered below the threshold voltage where the leakage energy balances the active energy dissipation [3,4]. However, aggressive reduction of the supply voltage significantly degrades the nominal performance and increases the circuit performance variation. Compared to deep sub-threshold operation, near-threshold operation has been considered to be more practical due to substantially improved performance and variation with comparable energy reduction [5–7]. Future low-power systems-on-chip (SoCs) are likely to consist of many voltage domains scalable from near-threshold to super-threshold region. This requires level shifters to be able to perform fast and energy-efficient level shifting for a wide range of supply voltages from near-threshold to super-threshold region [5,8–10].

Two types of conventional level shifters for super-threshold level shifting are shown in Fig. 1. The type I is based on cross-coupled PMOS structure. M_{P1} and M_{P2} form the cross-coupled structure and maintain the output at V_{DD} or ground. M_{N1} and M_{N2} are usually sized larger than M_{P1} and M_{P2} in order to flip the output as the input level is lower than the output level. This structure works for input levels well above the threshold voltage. As the input level approaches the threshold voltage, M_{N1} and M_{N2} are nearly turned off. The pull-down current is unable to overcome the pull-up current and the circuit fails to flip. A straightforward solution is to increase the size of M_{N1} and M_{N2}. This is however impractical because when the input level is close to the threshold voltage M_{N1} and M_{N2} conduct sub-threshold current which is far smaller than the super-threshold current flowing through M_{P1} and M_{P2}. For example, simulation in 90-nm technology shows that M_{N1} and M_{N2} have to be sized around 2000 times larger than M_{P1} and M_{P2} for the operation in near-threshold region [11]. Different from the type-I level shifter, the type II employs current mirror structure to achieve level shifting. When the input is high, there is current flowing through M_{N1} and M_{P1}. This results in amplified mirror current in M_{P2}, which charges the output to high. When the input is low, the mirror current is disabled and the output is discharged to low by the current through M_{N2}. This circuit can operate at lower input level. But its problem is that when the output is high, there is a constant static current path through M_{P1} and M_{N1} leading to large standby leakage power.

In this paper, two fast and energy-efficient level shifter designs with wide operating voltage range from near-threshold to super-threshold region are proposed. They are based on type-I and type-II structures, respectively. Both of the proposed level shifters show significantly better performance and energy efficiency than the state-of-the-art designs with similar or less area. One of them is slightly faster while the other occupies slightly less area. They are all suitable for level conversion in low-power systems with multiple scalable voltage domains. In Section 2, the state-of-the-art level shifters are reviewed. Section 3 presents the proposed two level shifter designs. Section 4 shows the simulation results and

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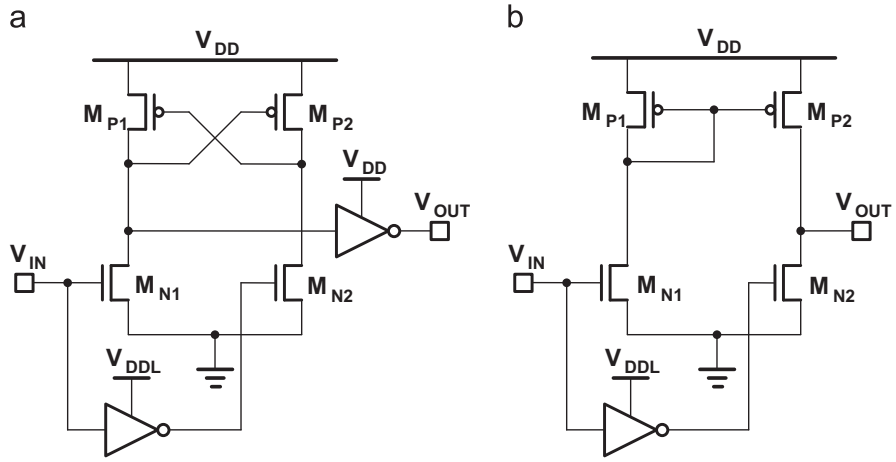

Fig. 1. Conventional level shifters. (a) Type I based on cross-coupled PMOS transistors and (b) type II based on current-mirror structure.

comparison between the proposed and current state-of-the-art level shifters. In Section 5, conclusions are drawn.

2. State-of-the-art level shifters

Over the past few years, many level shifter designs have been proposed to overcome the problems of the conventional level shifter structures discussed in Section 1. Among the state-of-the-art level shifters, the structure presented in [12] uses reduced swing inverter (RSI) to weaken the pull-up path in the type-I structure to achieve fast transition without extremely upsized pull-down transistors. However, the structure uses more than 20 transistors which increase its area consumption and sensitiveness to process variation. Another drawback is that the propagation delay does not scale with voltage very well as the pull-up transistors are constantly weakened.

In [13], as shown in Fig. 2(a), a diode-connected NMOS transistor is employed to weaken the pull-up network in the type-I structure and two cascaded level-shifting stages are used to achieve full swing. Similar to the RSI-based level shifter, its propagation delay does not scale with voltage especially when the input voltage is well above the threshold voltage because the voltage drop across the diode-connected NMOS transistor is nearly constant. Consequently it may not be suitable for applications using dynamic voltage scaling (DVS). Another drawback is significantly asymmetric rise and fall delay especially at ultra low voltages due to lower transconductance of the cross-coupled PMOS transistors at high-to-low transition caused by the input inverter delay.

The design in [10] achieves fast level shifting by creating non-conflicting rise and fall transitions with feedback control based on the type-I structure. The disadvantage of this circuit is large size of pull-down transistors and increased active energy due to stacking transistors in the weak pull-down path which makes it even weaker. The asymmetry between the pull-up and pull-down paths may also cause the circuit to lose its balance of rise and fall delay or even fail at low voltages.

A modified type-II level shifter is proposed in [11] as shown in Fig. 2(b). Unlike the design shown in Fig. 1(b), it uses a feedback control to disable the static current path and reduce standby leakage power when the output is high. However, disabling the static current path leads to a voltage drop for the high output caused by the reduced mirror current. This may create another static current path in the subsequent buffering circuit. Another drawback is that the pull-up transistor M_{P2} is partially on for the low output, which increases the standby leakage power and fall delay. Increasing the size of the pull-up transistor may reduce the

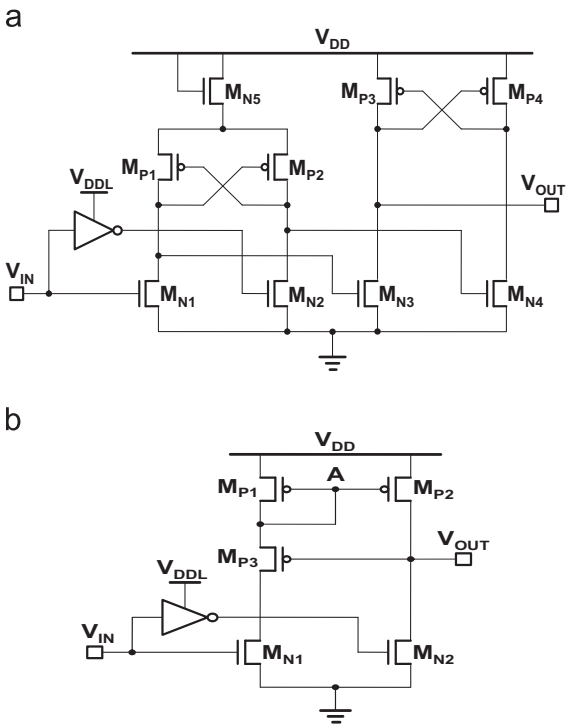

Fig. 2. State-of-the-art level shifters. (a)Two stage type-I level shifter with a diode-connected NMOS between V_{DD} and cross-coupled PMOS transistors [13]and (b) type-II level shifter with reduced static current leakage [11].

voltage drop and standby leakage for the high output, but it will increase the leakage for the low output and the fall delay due to the strengthened pull-up path.

In [14], a forward body bias is applied to the pull-down transistors in the type-I level shifter to reduce the propagation delay during transitions and a reverse body bias is applied to reduce the standby leakage when no transition occurs. The main drawback is the large area overhead caused by the well separation, body bias control, and output detection. Moreover, this method requires a triple-well process technology and the forward body biasing itself consumes leakage power.

3. Proposed level shifters

By carefully examining the advantages and disadvantages of the existing designs, we propose two new level shifter structures

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