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An LP/CBP reconfigurable analog baseband circuit for software-defined radio receivers in 65 nm CMOS

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ABSTRACT

A low pass (LP) and complex band pass (CBP) reconfigurable analog baseband circuit for software-defined radio (SDR) receivers is presented. It achieves 1–15 MHz LP bandwidth, 2–8 MHz CBP bandwidth and 0–36 dB gain range with 1 dB step. Nulling-resistor Miller feed-forward (NRMFF) differential-mode compensation, passive left half-plane (LHP) zero common-mode compensation and Quasi-Floating Gate (QFG) technique are proposed to improve the high frequency performance and driving capability of the embedded fully differential operational amplifier (Op-Amp). The analog baseband circuit has been implemented in 65 nm CMOS. It achieves 15.2 dB m/27.1 dB m IB/OB-IIP3, −2 dB m IP1dB and 71 dB m IIP2 while consuming 3.6–9.1 mW from a 1.2 V power supply and 0.75 mm^2 chip area.

1. Introduction

Along with the rapid development of wireless communication, one radio supporting multiple communication standards or/and multiple communication modes is greatly demanded. One approach to reach this goal is to utilize the SDR receivers [1–4], in which the hardware could be reconfigured with the software to support various wireless applications. Most of the reported receivers [3,4] adopt the zero-IF architecture to support wideband cellular communications. However, for wireless narrow-band applications such as GSM and ZigBee, low-IF architecture [5] may be more suitable. Therefore, the zero-IF/low-IF reconfigurable architecture is a more suitable solution to the real SDR receivers which should support not only the wireless wideband application, but also the wireless narrow-band applications.

Although many analog baseband circuits have been presented in the literatures to support zero-IF or low-IF receivers, there are few analog basebands which can be used for zero-IF/low-IF reconfigurable receivers. Horng-Yuan et al. [6] introduce a 250 MHz analog baseband circuit for ultra-wideband zero-IF receivers, where the programmable gain amplifiers (PGAs) and the filters are implemented with current-mode amplifiers to achieve wide bandwidth and wide dynamic range.The study in [7] presents a 5th-order programmable active-*RC* filter for LTE receivers. It can support reconfigurable low-pass bandwidth between 0.7 MHz and 10 MHz. A low-IF analog baseband chain [8] is proposed for ZigBee receivers, which includes a variable gain complex channel filter with 0.4–3.74 MHz signal bandwidth. A dual-mode complex band pass filter [9] is introduced to support low-IF Bluetooth/ZigBee receivers. In this paper, a low pass and complex band-pass analog baseband circuit is proposed to support zero-IF/low-IF reconfigurable SDR receivers.

One of the key building blocks in the analog baseband circuit is the Op-Amp. An analog baseband circuit based on the nulling-resistor Miller feedback (NRMFB) compensation Op-Amp is proposed for the SDR receivers in [10]. However, the Op-Amp need consume more power to extend its GBW to support wideband applications. Recently, the Miller feed-forward (MFF) compensation technique [11] is proposed to improve the Op-Amp bandwidth while reducing the power consumption. However, this technique reduces the GBW of the Op-Amp and deteriorates its stability. Furthermore, the Class-A Op-Amp [10] could not drive large capacitive load. Although Class-AB output stage [3] can improve the driving capability, one feedback loop is needed to improve the linearity, which increases the static power dissipation and circuit complexity. In this paper, a novel fully differential Op-Amp with NRMFF differential-mode compensation, passive LHP zero common-mode compensation and a Quasi-Floating Gate technique is proposed to improve its high frequency performance and driving capability while maintaining low power consumption.

The paper is organized as follows: the architectures of the SDR receiver and the analog baseband circuit are described in Section 2. In Section 3, the novel fully differential Op-Amp is proposed to improve its high frequency performance and driving capability, and the NRMFF differential-mode compensation, passive LHP zero common-mode compensation and QFG technique are discussed in detail. The LP/CBP reconfigurable analog filter and PGAs are

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introduced in Section 4. The current mode and voltage mode calibration circuits are introduced in Section 5 to calibrate the *I*/*Q* gain and phase mismatch. As the power control is critical for the SDR receivers, the wide dynamic range and high detection sensitivity received signal strength indicator (RSSI) is proposed to detect the signal strength in Section 6. Finally, Section 7 gives out the measured results and Section 8 draws some conclusions.

2. Architecture descriptions

2.1. SDR receiver architecture

The SDR receiver could be reconfigurable into either the zero-IF or low-IF architecture as shown in Fig. 1. The down-conversion system consists of a 25% duty-cycle voltage-mode passive mixer, a scalable trans-conductance amplifier and a flexible Tow-Thomas 2nd-order trans-impedance amplifier. The following flexible analog baseband realizes the channel selection filtering and signal amplification. The SDR receiver includes one low-pass and complex band-pass reconfigurable continuous-time sigma-delta ADC, which has the advantages of high resolution and embedded anti-alias characteristics, to convert the analog signals into digital. For wideband applications, such as LTE, the SDR receiver is reconfigured into the zero-IF architecture with the baseband filter reconfigured into low pass mode. While for narrow band communication, such as GSM, the low-IF architecture is adopted with the baseband filter reconfigured into the complex band-pass mode.

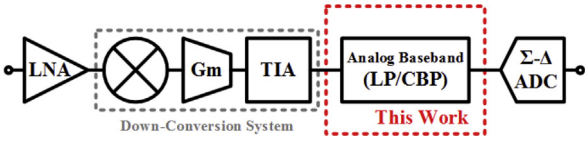

Fig. 1. The architecture of the SDR receiver.

2.2. Flexible analog baseband architecture

The flexible analog baseband architecture is shown in Fig. 2, which consists of a LP/CBP reconfigurable filter with 1–15 MHz LP bandwidth or 2–8 MHz CBP bandwidth, a two-stage PGA with 0–36 dB gain dynamic range and 1 dB gain step. To calibrate the *I*/*Q* gain and phase mismatch, two current-mode/voltage-mode calibration circuits are integrated. To overcome the effects of the process, power supply and temperature (PVT) variations, DC offset cancellation (DCOC) loop, digitally-assisted filter tuning are implemented, too. Besides, high sensitivity and high dynamic RSSI along with ADC and AGC loop are integrated together.

3. Fully differential Op-Amp design

The performance of the analog baseband circuits is mainly dependent on the high frequency performance and driving capacity of the embedded Op-Amp unit, which must be traded-off between the power consumption and the performance. Several techniques are proposed to improve the differential-mode and common-mode high frequency performance and the driving capacity of the Op-Amp unit.

3.1. Fully differential Op-Amp

As shown in Fig. 3, the fully differential Op-Amp consists of one input stage, one output stage and one common mode feedback stage. Miller feedback resistor R_C and capacitor C_C are served as NRMFB to improve the differential-mode phase margin. Miller

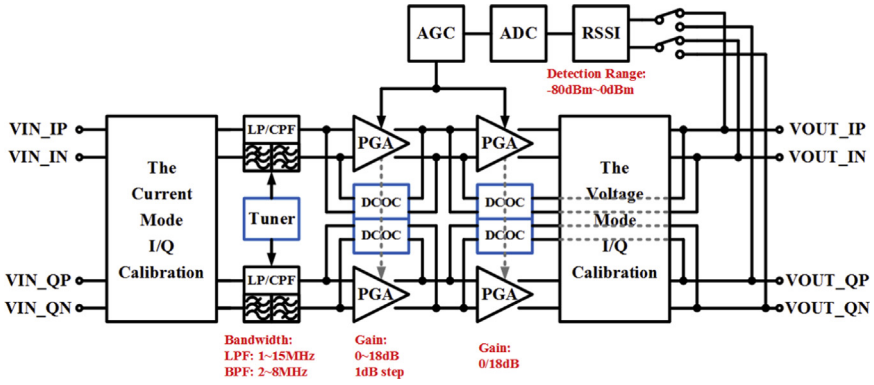

Fig. 2. The architecture of the flexible analog baseband.

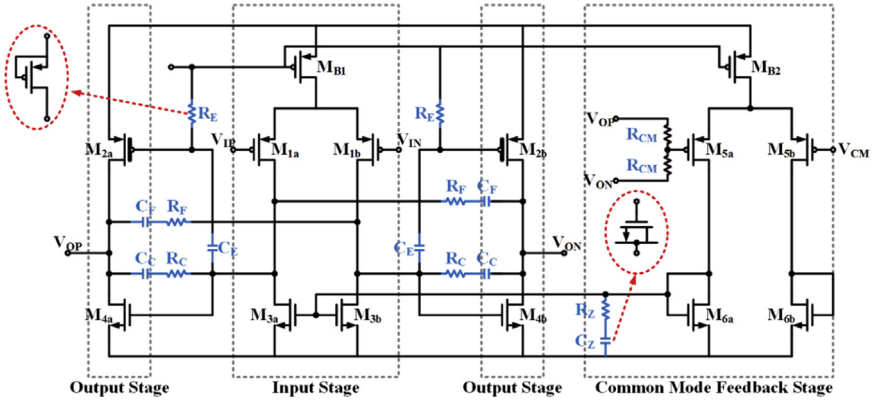

Fig. 3. The schematic of the fully differential Op-Amp.

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