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A resistive-feedback LNA in 65 nm CMOS with a gate inductor for bandwidth extension

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ABSTRACT

In order to get a wideband and flat gain, a resistive-feedback LNA using a gate inductor to extend bandwidth is proposed in this paper. This LNA is based on an improved resistive-feedback topology with a source follower feedback to match input. A relative small inductor is connected in series to transistor's gate, which boosts transistor's effective transconductance, compensates gain loss and then leads the proposed LNA with a flat gain and wider bandwidth. Moreover, the LNA's noise is partially inhibited by the gate inductor, especially at high frequency. Realized in standard 65-nm CMOS process, this LNA dissipates 12 mW from a 1.5-V supply while its core area is 0.076 mm^2. Across 0.4–10.6 GHz band, the proposed LNA provides 9.5 ± 0.9 dB power gain (S_{21}), better than -11-dB input matching, 3.5-dB minimum noise figure, and higher than -17.2-dBm $P_{1\ dB}$.

1. Introduction

Up to now, to meet various applications, many wireless standards have been developed, such as digital video broad-casting (450–850 MHz), Wi-Fi (2.4/5.2 GHz), and UWB communication (3.1–10.6 GHz). To realize multiple standards and features on single chip is always attractive for its low power, low cost and small size. For that goal, multiband receivers are indispensable. The low noise amplifier (LNA), as the first block in receiver chain, plays a key role. Zargari et al. stacked several *LC*-tuned LNAs to cover narrow desired bands, which consumed large area and complicated receiver's design [1]. Reconfigurable LNA can share hardware to reduce area and power, but it cannot simultaneously deal signals of multiple bands [2]. The concurrent dual-band LNA proposed in [3] requires several bulky on-chip inductors to realize specific *LC* networks. Today, wideband LNAs which can accommodate multiple standards as well as reduce area and cost attracts more and more attention.

Usually, in order to improve product competitiveness, CMOS is preferable due to its high integration and low cost. But its large parasitic capacitance limits the bandwidth of LNA. Distributed amplifier can break the limit of GBW and achieve superior bandwidth at the cost of area, power consumption and NF which then limits its widespread use [4]. Inductive peaking at the load terminal [5] is another famous technique to effectively expand LNAs' bandwidth, but usually needs a very large inductor [6]. In this paper, inductive peaking at the input terminal is utilized to extend a resistive-feedback LNA's bandwidth. A relative small inductor is connected to LNA's input node, which can lead to an increasing transconductance with frequency. Thus, the gain loss due to load capacitance is compensated and a wider bandwidth and flat gain can be obtained. In addition, the LNA's noise performance also benefits from the gate inductor. In this paper, the LNA's performance such as voltage gain, input matching, NF and linearity are discussed.

The paper is organized as follows. Section 2 reviews two basic resistive-feedback LNAs. Section 3 analyzes the proposed LNA and Section 4 provides a design guide with simulation results. Measured results and comparisons to other literatures are shown in Section 5. And finally, Section 6 concludes this paper.

2. Review of basic resistive-feedback LNA

The most common resistive-feedback LNA is shown in Fig. 1(a), and Fig. 1(b) gives an improved topology which reuses the PMOS current source to reduce power and noise. In short channel process, the input impedance and voltage gain of the LNA in Fig. 1(b) are expressed as:

$$Z_{in} = \frac{r_{on} \| r_{op} + R_f}{1 + (g_{Mn} + g_{Mp})(r_{on} \| r_{op})} \quad (1)$$

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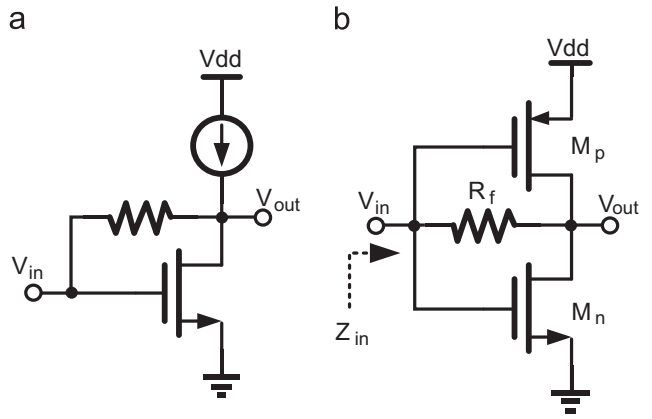

Fig. 1. Traditional resistive-feedback LNA, (a) with a current source just for DC-bias, (b) with a reuse PMOS current source.

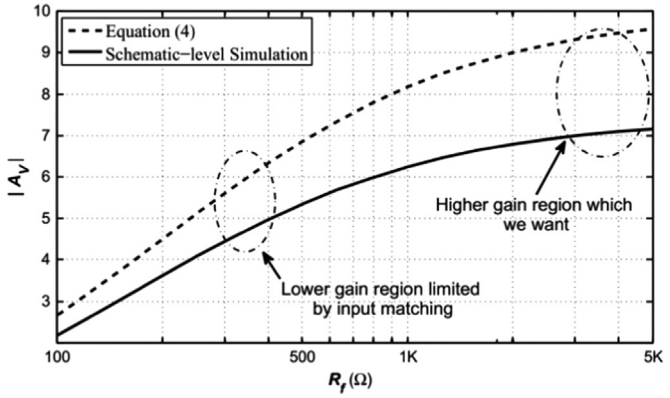

Fig. 2. Voltage gain versus R_f. The solid line is gotten from (2) with the assumption of $g_m r_o = 10$, the dashed line is from simulation in 65-nm CMOS, and both $g_{Mn}+g_{Mp}$ is 50 mS.

$$A_V = \frac{[1-(g_{Mn}+g_{Mp})R_f](r_{on} \| r_{op})}{R_f + r_{on} \| r_{op}} \tag{2}$$

where g_{Mn} and g_{Mp}, r_{on} and r_{op} are the transconductance and output resistance of M_n and M_p respectively. For 65-nm CMOS, transistor's intrinsic gain is about 10, i.e., $g_m r_o = 10$. If we assume $g_{Mn}+g_{Mp}$ is on the order of 50 mS (for the consideration of NF), R_f should be set to 350 Ω to match input to 50 Ω. As a result, the voltage gain is just about 6. Fig. 2 presents the calculated and schematic-level simulated voltage gain versus R_f. In order to match input, R_f is always restricted to a small value, which leads to a low gain.

Compared to traditional resistive-feedback LNA, the modified topology shown in Fig. 3 can alleviate the tie between input matching and gain, by using a source follower feedback path to match input [7]. The self-biased invertor (composed of M_1, M_2, and R_1) is only used to amplify signal, and R_1 just affords DC-bias and can be adjusted to a very large value to obtain a high gain as shown in Fig. 2. For convenience, we denote the LNA with source follower as SF-LNA and its voltage gain, input impedance, and NF are given below.

2.1. Voltage gain

Based on small signal model, the voltage gain of SF-LNA in Fig. 3 is derived as:

$$A_V = \frac{[1-R_1(g_{M1}+g_{M2})]\cdot(r_{o1} \| r_{o2})}{R_1 + (1+j\omega C_L R_1)\cdot(r_{o1} \| r_{o2})} \approx -A_0/(1+j\omega/\omega_p) \tag{3}$$

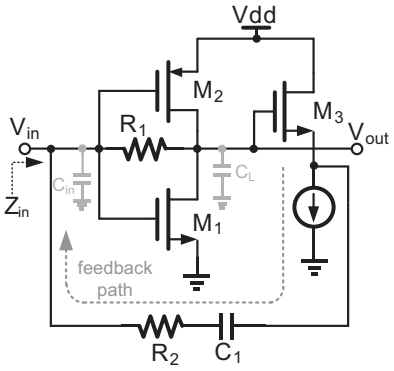

Fig. 3. Resistive-feedback LNA with source follower (SF-LNA).

where C_L is the total load capacitance, $\omega_p = 1/[C_L(r_{o1} \| r_{o2})]$, $A_0 = (g_{M1}+g_{M2})\cdot(r_{o1} \| r_{o2})$, and the approximate value is obtained with the assumption of $R_1 \gg r_{o1} \| r_{o2}$. Clearly, A_0 is the low frequency gain, and ω_p is the one-order pole.

2.2. Input impedance

Due to the large value of R_1, the input impedance of self-biased invertor is dominated by C_{in}, which includes M_1 and M_2's gate-source capacitance and equivalent gate-drain Miller capacitance. So, SF-LNA's input impedance can be expressed as

$$Z_{in}(\omega) = \frac{R_2 + g_{M3}^{-1}}{1-A_V} \Big\| \frac{1}{j\omega C_{in}}. \tag{4}$$

and the corresponding admittance is

$$Y_{in}(\omega) = \frac{(1+A_0)\omega_p^2 + \omega^2}{(R_2 + g_{M3}^{-1})(\omega_p^2+\omega^2)} + j\omega\left[C_{in} - \frac{A_0\omega_p}{(R_2+g_{M3}^{-1})(\omega_p^2+\omega^2)}\right]. \tag{5}$$

When ω is far below ω_p, we get

$$\frac{1}{\mathrm{Re}\{Y_{in}\}} = \frac{R_2 + g_{M3}^{-1}}{1+A_0} \tag{6}$$

and this can be set to signal source impedance, R_s. Through observing the imaginary part of (5), SF-LNA's equivalent input capacitance can be given as follows:

$$C_{eq} = C_{in} - \frac{A_0\omega_p}{(R_2+g_{M3}^{-1})(\omega_p^2+\omega^2)}. \tag{7}$$

It is clear that C_{in} is partially canceled and SF-LNA is a kind of reactance-cancelling LNA [8]. When ω goes high, the effect of reactance-cancelling can be omitted and C_{eq} approaches to C_{in}.

2.3. Noise figure

To analyze SF-LNA's noise characteristic, the ideal current source in Fig. 3 is replaced by an NMOS transistor M_4, and the total noise factor is given by:

$$F = 1 + \left(1+\frac{1}{1+A_0}\right)^2\left[\frac{\gamma_1 g_{M1} + \gamma_2 g_{M2}}{R_s(g_{M1}+g_{M2})^2}\right] + \frac{R_2}{R_s(1+A_0)^2} + \frac{1}{R_s g_{M3}(1+A_0)^2}\left(\gamma_3 + \frac{\gamma_4 g_{M4}}{g_{M3}}\right) + \frac{[R_s + (g_{M1}+g_{M2})^{-1}]^2}{R_s R_1} \tag{8}$$

where γ_1, γ_2, γ_3 and γ_4 are the thermal noise coefficients of M_1, M_2, M_3 and M_4 respectively. Usually M_1 and M_2 are the main noise contributors and larger transconductance can lead to a better NF, a familiar tradeoff between NF and power.

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