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Analytical modeling and parameter extraction of top and bottom contact structures of organic thin film transistors

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ABSTRACT

This paper proposes a structure based model of an organic thin film transistor (OTFT) and analyzes its device physics. The analytical model is developed for the top contact structure by mapping the overlap region to the resistance (in the vertical direction) that includes the contact and the bulk sheet resistances. Total device resistance includes the vertical resistance per unit area of the contact region and the sheet resistance of the channel. In addition, the drain and the gate voltages take into account the potential drop across the respective contacts. The gate bias dependent mobility is considered in place of constant mobility, since; it is more realistic and relevant to the organic TFTs. The proposed analytical model is also applied to the bottom contact structure and the current–voltage (I–V) characteristics are obtained. Furthermore, a differential method is employed to extract the parameters, such as, mobility enhancement factor γ, threshold voltage V_T, mobility μ_B, characteristic length L_C, vertical resistance R_V and contact resistance R_C. Finally, the model is validated in terms of electrical characteristics and performance parameters for both top and bottom contact structures. The analytical model results are in close agreement with the experimental results.

1. Introduction

The performance of an organic thin film transistor (OTFT) has experienced an impressive improvement in recent years [1]. Organic materials are attracting significant interest for being employed as the channel, the dielectric layer and the contact in TFTs. The organic transistor offers robustness, low temperature fabrication and mechanical flexibility, which are beneficial for the backplane driver application of organic light emitting diode (OLED) display, sensors and radio frequency identification (RFID) tags [2–7]. They emerge as imperative and viable for low cost large area electronic flexible integrated circuits [8–11]. Noteworthy progress in the fabrication methodology has made them appropriate for commercialization; however, the contact effect still appears as a limiting factor [12–14]. The parasitic series contact resistance is the major issue that dominates the overall device performance especially at the short channel [15]. In using the typical MOSFET expressions for the current–voltage (I–V) characteristics of these transistors, one needs to consider the non-ohmic behavior of the contacts and the gate bias dependent mobility [16–19].

OTFT operates in the accumulation mode and the mobility depends on the gate voltage V_{GS}. In recent years, numerous mathematical models [20–35] were developed, based on mainly the classical MOS transistor model by introducing the empirical parameters. The contact resistance is generally estimated by employing the transmission line method (TLM), Kelvin probe microscopy and the gated four-probe system that shows the series and the contact resistances as a function of the gate voltage [18,22–25,33,35,36]. Charge localization and conduction occur at the semiconductor/insulator interface, as well as in the bulk of the organic semiconductor (OSC) [21,37–40]. Therefore, the gate-contact overlap region needs to be analyzed separately for an adequate understanding of the device operation [6,21,38].

This article analyzes an effective channel and an overlapping region, to develop the model for top contact structure. The device resistance includes the vertical resistance per unit area of the contact region and the sheet resistance of the channel. Furthermore, the drain and the gate voltages are incorporated, excluding the voltage drop across the contacts. Field dependent mobility is included and performance parameters are extracted by means of employing a differential method. The output and the transfer characteristics are also plotted for the bottom contact structure and a reasonable match with the experimental results is obtained for both the structures.

2. Device structure and contact effects

A TFT consists of a thin film of OSC, usually fabricated as an inverted structure with a gate (G) at the bottom. It can be

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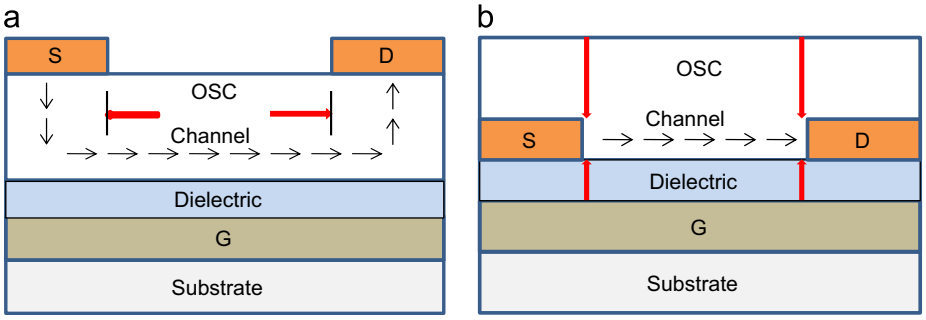

Fig. 1. The current flow path in (a) bottom gate top contact (BGTC) and (b) bottom gate bottom contact (BGBC) structures.

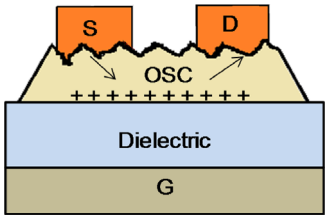

Fig. 2. Schematic for representing the access resistance and metal/OSC interface near the accumulation of holes in top contact OTFT.

classified as top or bottom contact, based on the relative position of the contacts with respect to the semiconductor. Source (S) and drain (D) contacts remain isolated from conducting channel in top contact, since they lie opposite side of the channel from the insulator. Traversing from S to D electrode, the charge carriers first travel downward followed by horizontal movement along the conducting channel and then proceed upward for extraction from the drain, as shown in Fig. 1(a). Traveling of charge carriers through a large area results in minimal contact resistance for such device [18].

In a bottom contact structure, contacts and dielectric layer are aligned on the same side of the induced channel [41]. Therefore, the carriers travel in a single plane due to the establishment of S/D connection directly with the channel [42–44] as shown in Fig. 1(b). The performance of these devices is usually observed to be inferior in terms of high contact resistance and low mobility. It is due to interface barrier and morphological disorders of semiconductor film around the pre-patterned S/D contacts [18,41,45]. However, OTFT in bottom contact structure is promising for low-end applications, since, it can be fabricated through spin coating, solution processing and simple printing techniques [16,36].

The main factor that results in high contact resistance of the top contact structure is the access resistance. It reduces due to large peak-to-valley roughness of the OSC film, which provides an easy flow of charge carriers, as depicted in Fig. 2 [44]. It can also be minimized using thinner OSC layers, but cannot be eliminated completely. Ideally, the contacts should be ohmic for enabling the whole applied voltage to the current conduction, as shown in Fig. 3(a). However, a significant amount of voltage drop is observed across the contacts, as shown in Fig. 3(b). In order to model this non-ohmic characteristic, the charge carrier's movement from S to D contact can be divided among three segments and each segment can be modeled with its respective resistance.

The source to channel segment is mapped to source resistance, R_S. Similarly, the region between channel and drain is modeled as drain resistance, R_D. Besides this, the channel resistance is designated as R_{CH}. Furthermore, the resistance linked to carrier injection and collection regions is collectively called contact resistance, R_C. Source and drain contacts' behavior is quite similar in most of the OTFT devices [18,20–22,46]. However, Burgi et al. demonstrated asymmetry between the two contacts, at a large Schottky barrier [47]. The main obstacle is generally observed in charge carrier injection at the source as compared to the extraction at the drain end [40]. While, both the contact resistances were found equal at a lower barrier height comparatively [47]. For simplicity, the obstruction to current flow is considered similar at both the contacts. Hence, the source and the drain resistances can be expressed as

$$R_S = R_D = R_C/2 \tag{1}$$

To analyze the combined effect of all three segments, the equivalent model can be represented by the source, the channel and the drain resistances in series, as shown in Fig. 4.

3. Analytical model of top contact OTFT

Modeling and parameter extraction of OTFT mainly rely on trends of output current, I_{DS} in a single crystalline MOSFET. Top and bottom contact devices exhibit the same working principle, but are different in terms of their fabrication and contact/series resistance that results in different I–V characteristics and mobilities [48,49].

Prior to the development of model, few points are taken into consideration, including, a uniform sheet resistance, $R_{SH}^{Channel}$ (Ω/square) across the channel and zero net bulk current in the semiconductor [6]. Accumulation of carriers is assumed at the bottom of the overlapping region as well as in the channel [50,51]. Usually, the contacts drop a significant amount of voltage, due to which the external applied voltages do not contribute entirely to the current conduction. Accordingly, actual channel ends are represented by terminals S′ and D′ rather than S and D, respectively, as shown in Fig. 4. Effective voltages are taken into account after excluding voltage drops across the contacts. Subsequently, the drain current is considered as a function of internal drain–source voltage V'_{DS} (between the terminals D′ and S′) and the gate–source voltage V'_{GS} (between the terminals G and S′), which are somewhat lesser than the external voltages V_{DS} and V_{GS}, respectively [4,6,28,46].

To derive the current–voltage model under these assumptions, channel and overlap regions are analyzed separately. The channel region is considered first and, thereafter, resistance in the overlapping region is amended. The drain current, analogous to internal voltages, V'_{GS} and V'_{DS}, both in linear [$V'_{DS} \le (V'_{GS} - V_T)$] and saturation [$V'_{DS} > (V'_{GS} - V_T)$] regions can be expressed as [28,46]

$$I_{DS}^{Lin} = \frac{Z}{L}\mu C_{OX}\left[(V'_{GS} - V_T) - \frac{V'_{DS}}{2}\right]V'_{DS} \tag{2}$$

$$I_{DS}^{Sat} = \frac{Z}{2L}\mu C_{OX}(V'_{GS} - V_T)^2 \tag{3}$$