



Novel and general carbon nanotube FET-based circuit designs to implement all of the 3^9 ternary functions without mathematical operations

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ABSTRACT

In this paper, we propose new universal designs of ternary-valued logic (TVL) with high-speed, low-power and full swing output using carbon nanotube FETs (CNTFETs). All of the TVL functions (3^9 functions) can be implemented in these designs. Ternary value logic is a promising alternative to binary logic due to the reduced integrated circuit (IC) interconnects and chip area. Therefore, a universal design of TVL is a good direction for the future of FPGA design using CNTFET. In this paper, new universal designs of ternary-valued logic based on CNTFETs are proposed and compared with the existing resistive-load CNTFET universal TVL designs. Extensive simulations have been performed in HSPICE to investigate the distribution of power consumption and the delay of the CNTFET-based universal cells due to variations in the supply voltage, the diameter of the CNT, and the room temperature. Simulation results show that the proposed universal TVL designs result in significantly lower power consumption and delay compared with previous resistive-load CNTFET universal TVL implementations.

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1. Introduction

Most computational operations today are performed with only two logical states (0 and 1). Multiple-valued logic (MVL) replaces the characterization of variables in the binary number system with higher-based systems such as ternary [1].

Ternary logic (or three-valued logic) (TVL) has attracted substantial interest due to several important advantages over binary logic in the design of digital systems [2,3]. For example, more information can be transmitted across the same communication channel or stored for a given register length. A reduction in chip area, the complexity of interconnections and power dissipation are some of the advantages that can be achieved [4]. Furthermore, serial and serial-parallel arithmetic operations can be performed faster, and more operative error-detection and error-correction codes can be employed in ternary logic implementations.

The carbon nanotube FET (CNTFET) alternatives to bulk silicon transistors are of particular interest. CNTFETs are promising for increased performance due to a unique one-dimensional band structure that displays near-ballistic transport and low OFF-current properties [2–10]. The design of a high performance universal TVL cell based on a CNTFET can result in low-power, fast-programmable logic circuit implementations such as CPLDs or FPGAs. Inefficient use of the chip area, low speed and high power consumption due to electronic

switches are major problems with programmable ICs. A universal TVL cell has been presented in [11]. In this paper, new designs using ternary valued-logic and nanoscale CNTFETs are proposed. Therefore, future programmable logic ICs with low power and high speed properties can be achieved with minimal chip area. Two universal TVL cells based on CNTFETs with a resistive voltage divider are proposed in this paper. We know that the resistor is an undesirable element in the manufacturing process of ICs due to high power consumption and large dimension. Hence, the voltage division is performed by two CNTFETs (i.e., a pass gate).

In the CNTFET, the threshold voltage of the transistor is determined by the carbon nanotube diameter. Therefore, different threshold voltages for CNTFETs can be implemented by growing CNTs with different diameters (chirality vector). This quality makes CNTFETs an ideal platform to bring MVL to electronic chips [12–17]. CNTFET-based universal TVL cell designs with optimized threshold voltages are proposed and compared to previous implementations of universal cells. Extensive simulations with HSPICE are performed to show the impact of supply voltage and room temperature variations. Simulation results show that the proposed universal TVL cell with pass gate voltage division has better performance in terms of power consumption and delay compared with previous designs.

2. Carbon Nanotube FET

CNTFETs using semiconductor single-wall carbon nanotubes (SWCNTs) are used to build electronic circuits. Their properties are

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similar to MOSFETs. A SWCNT is a cylindrical shape made by a simple mechanized processing device and is an extremely promising choice over current MOSFETs. Whether the SWCNT has metallic or semiconductor characteristics contributes to its electrical properties, which depend on the angular arrangement of atoms along the tube. This arrangement is based on a chirality vector with a pair of integers (m and n), i.e., the nanotube is metallic if $n=m$; otherwise, the tube is a semiconductor. The CNT diameter is calculated by eq. (1), which is a function of m and n [18]. Fig. 1 shows a diagram of the CNTFET [18].

$$D_{\text{CNT}} = \frac{\sqrt{3}a_0}{\pi} \sqrt{n^2 + m^2 + nm} \quad (1)$$

The threshold voltage has been defined as the voltage needed to turn the transistor on. The voltage of the CNT channel is approximately half of the band gap and is inversely related to the nanotube diameter [19].

$$V_{\text{th}} \approx \frac{E_g}{2e} = \frac{\sqrt{3}}{3} \frac{aV_{\pi}}{eD_{\text{CNT}}} \quad (2)$$

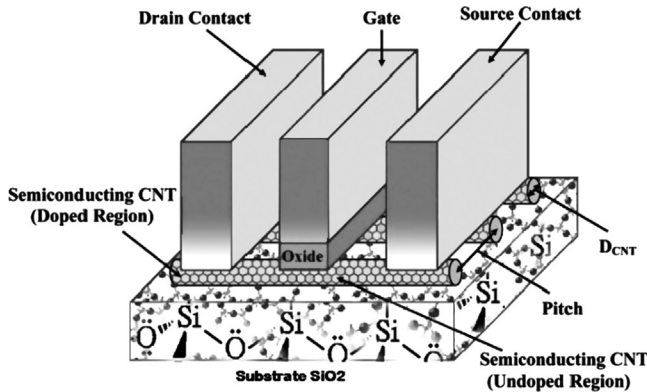


Fig. 1. Diagram of a carbon nanotube transistor.

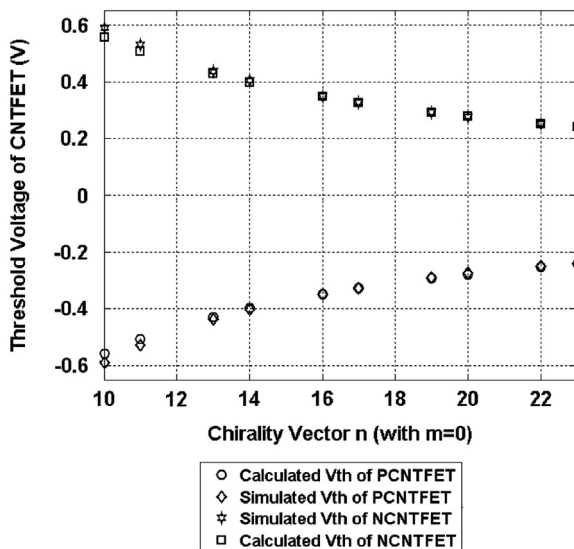


Fig. 2. Threshold voltage of CNTFETs versus n (for $m=0$).

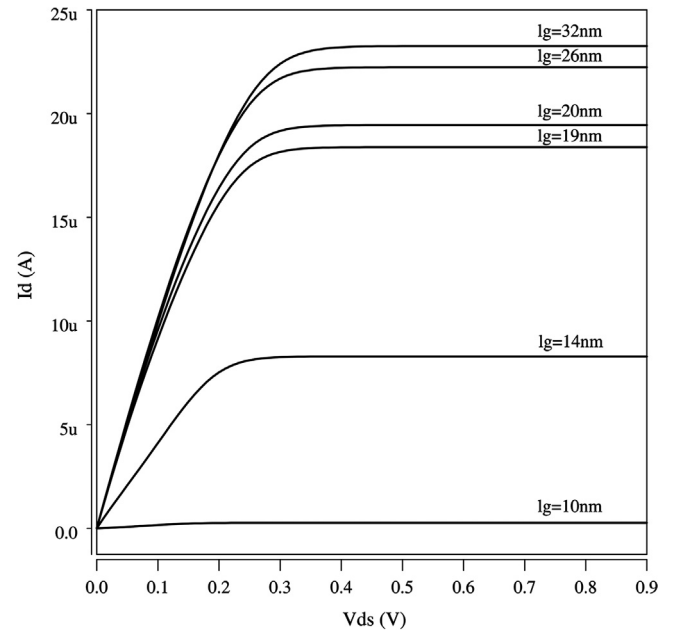


Fig. 3. Current-voltage (I - V) characteristics of a ballistic CNTFET.

D_{CNT} is the CNT diameter, e is the unit electron charge, $V_{\pi}=3.033$ eV is the carbon π - π bond energy in the tight bonding model, and $a=2.49$ Å is the carbon-to-carbon atom distance. For example, the threshold voltage of the CNTFETs that use (19, 0) CNTs as channels is 0.289 V because the D_{CNT} of a (19, 0) CNT is 1.49 nm. Simulation results have acknowledged the validity of this threshold voltage. Because the vector changes, the CNTFET threshold voltage will also change. The threshold voltage of the CNTFET is inversely related to the CNT chirality vector. The threshold voltage of the CNTFET using (13, 0) CNTs is 0.423 V, whereas the threshold voltage of the CNTFET by means of (19, 0) is 0.289 V. Fig. 2 shows the threshold voltage of both P- and N-type CNTFETs obtained from (2) and HSPICE simulation results for various chirality vectors (various n for $m=0$).

The current-voltage (I - V) characteristic of the CNTFET with different gate lengths is shown in Fig. 2, which shows that the I - V characteristics of the CNTFET are similar to those of the MOSFET. The CNTFET circuit current is saturated at higher V_{ds} (drain to source voltage) as the channel length increases, as shown in Fig. 3. The energy quantization in the axial direction at a 32-nm (or less) gate length causes the on-current to decrease, as expected [18].

3. Proposed designs

Two designs of universal TVL cells based on CNTFETs with high speed and low power consumption are presented. The first cell, with 16 N-type CNTFETs, is shown in Fig. 4. In this cell, voltage division is performed by two resistors, which increases the power consumption and makes the chip manufacturing process difficult.

Referring to the table of ternary logical functions (Table 1), we observe that each of the branches is used to achieve a state of the table.

For example, the branch named “i” is connected to ground if T1 and T5 are turned on. This means that inputs A and B are equal to “0”, which is implemented in the first step, according to the table. For a logical “0” in output, the related branch connects to “zero”, so we have “0” in the output. By changing to a logical “1”, the

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