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Novel pipeline architectures based on Negative Differential Resistance devices

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ABSTRACT

Devices exhibiting Negative Differential Resistance (NDR) in their *I–V* characteristic are attractive from the design point of view and circuits exploiting it have been reported showing advantages in terms of performance and/or cost. In particular, logic circuits based on the monostable to bistable operating principle can be built from the operation of two series connected NDR devices with a clocked bias. Monostable to Bistable Logic Element (MOBILE) gates allow compact implementation of complex logic function like threshold gates and are very suitable for the implementation of latch-free fine grained pipelines. This pipelining relies on the self-latching feature of MOBILE operation. Conventionally, MOBILE gates are operated in a gate level pipelined fashion using a four-phase overlapped clock scheme. However other simpler, and higher through-output interconnection schemes are possible. This paper describes latch-free MOBILE pipeline architectures with a single clock and with a two phase clock scheme which strongly rely on distinctive characteristics of the MOBILE operating principle. Both the proposed architectures are analyzed and experimentally validated. The fabricated circuits use a well-known transistor NDR circuit (MOS-NDR) and an efficient MOBILE gate topology built on its basis. Both solutions are compared and their distinctive characteristics with respect to domino based solutions are pointed out.

1. Introduction

Different emerging devices like Resonant Tunneling Diodes (RTDs), tunnel transistors or molecular RTD devices exhibit Negative Differential Resistance (NDR) in their *I–V* characteristic. Many working circuits taking advantage of it covering different applications and with different goals, including high speed, low power or reduced device count [1–3] have been reported using III–V technologies. Incorporation of RTDs into CMOS is currently a key target. Thus, developing design techniques exploiting NDR feature at different levels (circuit, architecture, etc.) is currently an area of active research. Moreover, exploration of transistor circuits that emulate the NDR characteristic has recently received renewed attention in order to incorporate the benefits of NDR based circuits into transistor technologies [4–10].

From the point of view of design, the NDR characteristic is very attractive. On one hand, it can be exploited in non-linear circuits like oscillators or frequency dividers. On the other, it is useful in the implementation of memories due to the existence of stable states associated to the inclusion of NDR elements. In particular, the Goto pair is well known [11]. The circuit consists of two NDR devices connected in series leading to three operating points, two stable and one unstable. The two stable points can be used to represent and store data. On the basis of the Goto pair, logic circuits which operation is based on a Monostable to a Bistable Logic Element (MOBILE) have been developed. MOBILE gates are implemented operating two series connected NDR devices with a switching bias. There is a pair of interesting characteristics of MOBILEs in comparison to conventional logic gate implementations.

First, they increase the functionality implemented by a single gate in comparison to MOS and bipolar technologies and, thus, circuit complexity. In particular, the operating principle of MOBILE is extremely well suited to implement the arithmetic operation on which threshold gates (TGs) are based [12]. Different topologies for MOBILE TGs and Multi-Threshold threshold gates have been reported and experimentally validated [13,14].

Second, the self-latching property of MOBILEs, arising from their NDR characteristic, allows the implementation of fine grain pipelines which can be achieved without resorting to memory elements [1,15]. In this way, exploration of interconnection schemes for MOBILE gates is relevant for the design of functional units for high performance applications.

Originally, it was proposed to operate MOBILE gates in a gate level pipelined fashion using a four-phase overlapped clock scheme. Conventional counterpart of this super-pipelining is the

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operation of Domino dynamic logic in a pipelined fashion using an overlapping multi-phase clock scheme and without latches between consecutive clock phases [16]. Variations of this multi-phase domino solution (three to six phases) have been developed by different companies and applied into commercial circuits [17,18]. However, MOBILE pipelines do not exhibit the functional limitation of domino solutions, and thus, both inverting and non-inverting blocks can be chained.

The overcoming of the functional limitation is not the only advantage of the MOBILE architectures, but their edge-triggered feature allows the implementation of other distinctive interconnection schemes. In particular, this characteristic can be exploited to reduce the number of clock-phases, which is attractive both from the point of view of increasing through-output, and for simplifying clock distribution. In addition, MOBILE naturally suits gate-level pipelined operation which also increases through-output. In this sense, dynamic logic based gate-level pipelined architectures, with one or two clock phases, are being also explored but at the expense of incorporating latches [19,20].

In addition to the exploration of distinctive interconnection schemes, other previous papers have focused the assessment of the performance advantages of the RTD-based MOBILE pipelines technology with respect to conventional dynamic-logic based ones. In [21] it is reported that tunnel diodes improves speed, by a factor between 1.2 and 2.3 and reduces active power, by a factor between 1.5 and 1.8, with respect to dynamic logic. In [22] RTD-based MOBILE gate-level pipelines are shown to be significantly more power efficient than conventional dynamic CMOS, with power ratios over 2 in most of the reported comparison experiments and with larger ratios in some of them.

This paper describes latch-free MOBILE pipeline architectures with a single clock and with a two phase clock scheme which strongly rely on distinctive characteristics of the MOBILE operating principle. The analysis both qualitative, examining the distinctive behavior of the proposed MOBILE pipelines with respect to the dynamic based ones, as well as quantitative, deriving timing constraint, and the experimental validation are main aims of the paper. For the later, we have resorted to well-known 3-transistor topology exhibiting NDR. Prototypes of both architectures have been designed, fabricated and tested in a commercial CMOS technology.

The paper is organized as follows: in Section 2, MOBILE logic style is described. In Sections 3 and 4, we describe and analyze the single phase and the two-phase MOBILE pipelines, respectively. Section 5 shows experimental results validating their operation and compares both the approaches. Finally, some key conclusions are given in Section 6.

2. MOBILE operation principle

2.1. MOBILE logic gates

The MOBILE [12] in Fig. 1a is an edge-triggered current controlled gate which consists of two devices exhibiting NDR in their *I–V* characteristic (Fig. 1b), connected in series and driven by a switching bias voltage, V_{CK}. When V_{CK} is low, both NDRs are in the on-state and the circuit is monostable. Increasing V_{CK} to an appropriate maximum value ensures that only the device with the lowest peak current switches from the on-state to the off-state. Output is high if the driver NDR switches and it is low if the load does. Logic functionality can be achieved if the peak current (I_P in Fig. 1b) of one of the NDR devices is controlled by an input. In the configuration of the rising edge-triggered inverter MOBILE shown in Fig. 1c, the peak current of the driver NDR can be modulated using the external input signal V_{in}. Transistor behaves like a

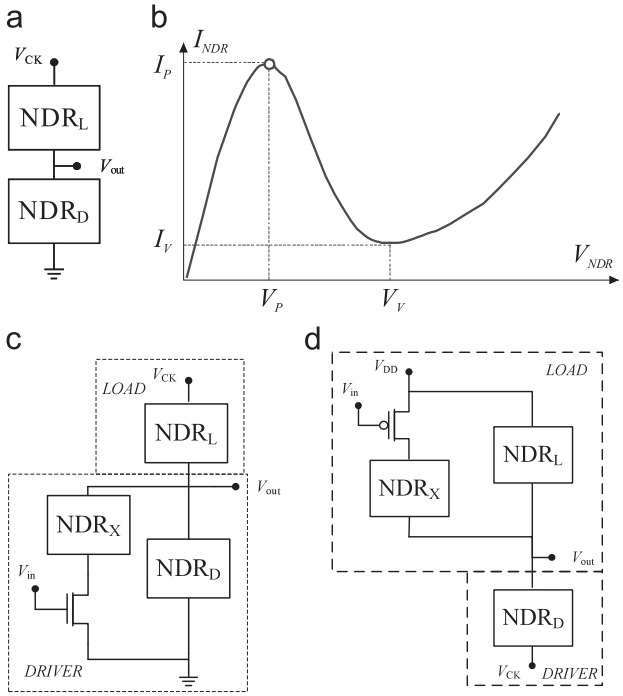

Fig. 1. MOBILE circuits: (a) MOBILE; (b) NDR *I–V* characteristic; (c) rising edge-triggered MOBILE inverter; and (d) falling edge-triggered MOBILE inverter.

switch, so that for a low input, current flows only through NDR_D, but for a high input, the effective peak current of the driver is the sum of the peak currents of NDR_D and NDR_X. More complex logic functionality can be implemented in two different ways. Clearly, replacing the single transistor in Fig. 1c by an NMOS transistor network, other logic functions are implemented. NDR peak currents are selected such that the value of the output depends on whether the network transistor evaluates to "1" or to "0". Alternatively, topologies for implementing threshold functions[1] [23] have been proposed [12]. The inverter shown in Fig. 1c can be also explained as a threshold gate, with a single input with associated weight $w_1=-1$ and threshold $T=0$. Adding input branches (NDR device plus transistor) in parallel to the driver (load) NDR inputs with negative (positive weights) are implemented. That is, the weighted sum and the comparison to a threshold value which defines the operation of a threshold gate are realized by means of the current controlled switching principle of the MOBILE.

Fig. 1d depicts a falling edge triggered inverter. Note that branch implementing functionality is now in parallel to the load NDR and uses a p-type transistor.

It is well known that a sufficiently slow V_{CK} rising (or falling) is required for MOBILE operation [24]. That is, there is a critical rise time for the switching bias below which the gate does not operate correctly. Under that critical rise time, there is at least one input combination for which the gate does not produce the expected logic output. It is due to AC currents associated to internal parasitics and output capacitive loads (fan-out), which are more important for faster clock changes, that somewhat "alter" the ideal MOBILE operating principle based on peak currents comparison. This critical value depends on both the circuits (NDR peak currents, fan-out, etc.) and technological parameters. That is, design requires taking into account this AC currents in order to

[1] A threshold gate (TG) is defined as a logic gate with n binary input variables, x_i ($i=1,...,n$), one binary output y, and for which there is a set of ($n+1$) real numbers: threshold T and weights w_1, w_2, ..., w_n, such that its input–output relationship is defined as $y=1$ if $\sum_{i=1}^{n} wixi \geq T$ and $y=0$ otherwise. Sum and product are the conventional, rather than the logical, operations.