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Advanced etching of silicon based on deep reactive ion etching for silicon high aspect ratio microstructures and three-dimensional micro- and nanostructures

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Abstract

Different processes involving an inductively coupled plasma reactor are presented either for deep reactive ion etching or for isotropic etching of silicon. On one hand, high aspect ratio microstructures with aspect ratio up to 107 were obtained on sub-micron trenches. Application to photonic MEMS is presented. Isotropic etching is also used either alone or in combination with anisotropic etching to realize various 3D shapes.

Keywords: Micromachining; DRIE; HARMS; Sub-micron; 3D; Silicon

1. Introduction

Less than 10 years ago, inductively coupled plasma (ICP) reactors have been introduced for silicon reactive ion etching (RIE) process leading to the deep reactive ion etching (DRIE) technique. The main novelties on these rather new ICP-RIE systems are the following:

- Separation of the main plasma from the wafer
- A higher plasma density
- Improved Radio Frequency RF-power supply
- Improved performance for pumping and mass-flow systems
- Pulsed Low Frequency LF substrate biasing
- New chemistry and new process (Bosch and cryogenic)

These hardware and process novelties led to improved performances, for instance:

- Higher selectivity for deep etching (DRIE)
- Higher aspect ratio (AR)
- Higher etching rate, either for anisotropic or isotropic etching
- Reduction of parasitic effects: notching, aspect ratio dependent Etching (ARDE), etc

The microfabrication of high aspect ratio microstructures (HARMS) is the main benefit of these technologies with numerous applications in the field of MEMS. There are two main ways of achieving HARMS by DRIE. The most popular way is the 'Bosch process', a patented process developed by Robert Bosch GmbH [1], which is based on alternating multiple steps of etching and sidewall passivation. The main alternative is the 'cryogenic process', relying on cooling the stage and silicon to cryogenic temperatures using liquid nitrogen [2,3]. In this work, both processes are studied, sometimes in isotropic conditions, in order to obtain unusual shapes or unusual feature sizes.

2. Sub-micron HARMS

2.1. Ultra-high aspect-ratio (AR) on sub-micron-wide trenches

Motivated by the need of fabricating silicon HARMS for nanophotonic applications [4,6], we developed a technological process for manufacturing deep trenches

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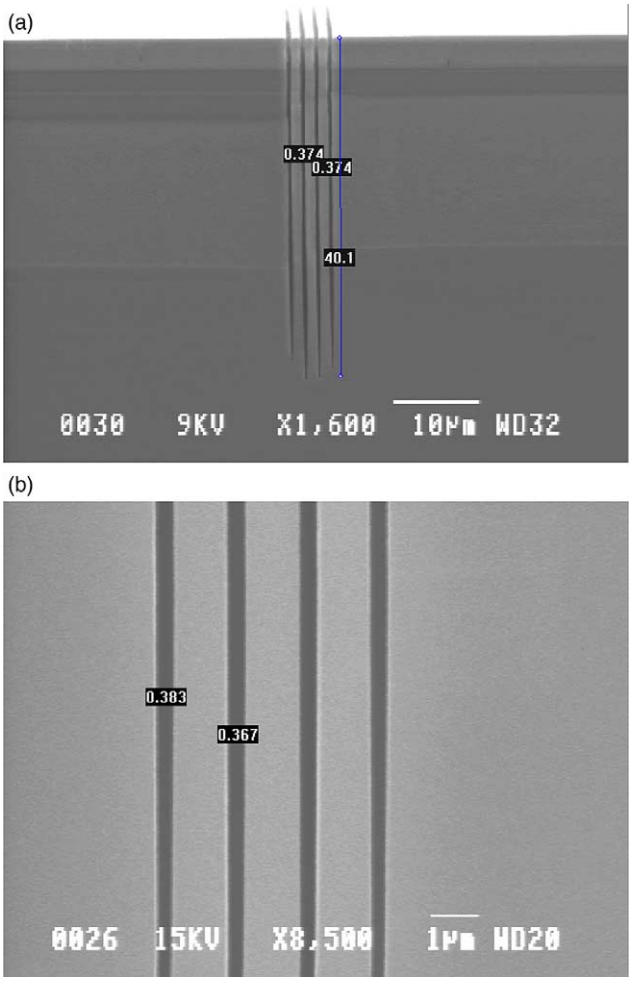

Fig. 1. (a) Silicon sub-micron deep trenches obtained by DRIE. Evidence is given of 0.374 μm—wide, 40.1 μm—deep trenches, corresponding to an aspect ratio of 107, (b) detailed view.

and holes as well as silicon walls and pillars having sub-micron feature sizes.

All our DRIE experiments were performed on an ALCATEL 601E System. Fig. 1 shows our latest results related to deep etching of sub-micron trenches. One can see 0.374 μm—wide, 40.1 μm—deep trenches, corresponding to an aspect ratio of 107. To our knowledge, this value of the aspect ratio is at the moment the highest ever obtained using a DRIE process.

The high aspect ratio micro- and nanostructures under consideration are obtained from three main process steps. First electron-beam (EB) lithography is performed in order to pattern nanostructures on an aluminum thin film layer, having a thickness of typically 200 nm. Then aluminum is etched using a chlorine-based chemistry in a conventional reactive ion etching (RIE) system. The third step consists of silicon deep etching with aluminum as a hard mask.

An ICP-RIE plasma etcher (Alcatel 601E) is used for this purpose. This equipment is configured with an ICP Radio Frequency source of 2 kW and a low frequency generator, for wafer polarization. Wafer is clamped with a mechanical chuck. In the experiments presented in this paper, the wafers were maintained at a temperature of 20 °C.

HARMS with openings in the range of 0.3–1 μm are obtained by tuning key parameters such as pressure, bias voltage and gas switching (SF_6/$C4F_8$). In order to achieve important depth, strong ion bombardment is needed. This ion bombardment also drastically affects the mask/Si selectivity. Therefore, photoresist or other soft mask materials cannot be used for this kind of experiments. Moreover, etching time for a sub-micron feature size is quite long due to ARDE effect. Typical etching rates are below 1 μm/min. Using a 200 nm-thick aluminum mask, the bias voltage is adjusted to maximize ion bombardment without reaching the limit value that induce mask sputtering. The pressure is also maintained to a low value between 2 and 2.5 Pa.

It is noteworthy that the developed process is specific to patterns of small dimensions only. Black silicon and excess of passivation appears on patterns with dimensions larger than 10 μm. Therefore, when a design requires the simultaneous fabrication of small openings (sub-micron) and large openings (10 μm and above), a two-mask approach should be used, in which etching of small features is separated from etching of large features.

2.2. Application of sub-micron HARMS to photonics

At the sub-micron scale, the roughness due to the scalloping introduced by the alternating (etching/passivation) steps of the Bosch process can be non-negligible. To minimize this effect, we set the switching time to a lower value than in conventional processes. The resulting peak-to-valley roughness can be reduced to 20 nm. Cryogenic process, which is expected to be more efficient in terms of surface quality of the sidewalls, was also studied as an alternative to optimized Bosch process. Examples of etching results using the cryogenic process are shown in Fig. 2.

The above-mentioned recent advances in the fabrication of sub-micron HARMS with high AR opens the way to new applications in photonics.

Among these applications to photonics one can mention the vertical distributed Bragg reflectors (DBRs) [4,5], which consist of alternating vertical silicon thin walls separated by thin air-gaps. Silicon and air are two materials with high index contrast (used namely in photonic crystals). These DBR's with vertical architecture form mirrors of high reflectivity with an optical axis in the plane of the substrate. Therefore, high quality, horizontal, Fabry–Pérot cavities are attainable. Moreover, association of these optical components with MEMS actuators is also possible using Silicon on insulator (SOI) substrates and it leads to new functionalities such as tunability and reconfigurability. An illustration of this is the tunable optical filter [5] shown in Fig. 3. It is noteworthy that the sub-micron HARMS with high AR also opens very promising application to devices based on photonic crystals.