Microelectronics Reliability 54 (2014) 2668–2674

Contents lists available at ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/microrel

Activation energy of drain-current degradation in GaN HEMTs under high-power DC stress

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ARTICLE INFO

Article history:
Received 9 July 2014
Received in revised form 26 August 2014
Accepted 15 September 2014
Available online 2 October 2014

Keywords:
GaN HEMT
Arrhenius
Activation energy
Degradation

ABSTRACT

We have investigated the role of temperature in the degradation of GaN High-Electron-Mobility-Transistors (HEMTs) under high-power DC stress. We have identified two degradation mechanisms that take place in a sequential manner: the gate leakage current increases first, followed by a decrease in the drain current. Building on this observation, we demonstrate a new scheme to extract the activation energy (E_a) of device degradation from step-temperature measurements on a single device. The E_a's we obtain closely agree with those extracted from conventional accelerated life test experiments on a similar device technology.

1. Introduction

In the last few years, high-voltage GaN FET technology has burst into the scene promising to revolutionize high-power high-frequency amplifiers as well as high-voltage power management systems [1–6]. A critical concern with this new technology is reliability [7–15]. This is particularly problematic due to the absence of a native substrate for GaN.

In this work, we study the role of temperature in the degradation of GaN HEMTs biased under high-power conditions, a topic that, in contrast with the OFF-state, has received little attention in spite of its importance for power amplifier applications. A key difficulty in high-power stress experiments is managing self-heating and carrier trapping which is temperature dependent [16,17]. Unless these issues are correctly handled, it is difficult to isolate the dominant degradation mechanism and obtain its activation energy (E_a). This is required before device lifetime projections to realistic operating conditions can be made. Deriving the E_a of degradation in particular is very time consuming as it requires long-term stress experiments in many devices. In the early stages of development of a new technology, this is also difficult as variations in device characteristics introduce significant ambiguity in the interpretation of the results.

We present here a new methodology to study the high-power degradation of GaN HEMTs. Our approach is based on *step-temperature experiments* in which constant electrical stress is applied at a certain temperature for a given length of time and periodically the temperature is increased in steps. In this way, and with appropriate care to minimize the effect of trapping, we show that the activation energy of the dominant degradation mechanism can be derived from measurements *on a single device*. The new technique that we propose here, while demonstrated under high-power stress conditions in GaN HEMTs, should be applicable to other regimes of operation and other devices. Our research also reveals a sequential degradation pattern for the gate and drain currents in a GaN HEMT under high-power bias at high temperature in long-term stress experiments. Gate current degradation takes place first. Only after the gate current increase has saturated, drain current degradation occurs in a temperature-activated manner.

This paper is an augmented description of the presentation made in [18].

2. Experiments

The devices used in this study are prototype packaged S-band single-stage MMICs using a GaN-on-SiC HEMT. The transistor features $L_g = 0.25$ μm and $W_g = 2 \times 280$ μm.

Testing is carried out in an Accel-RF life-test system equipped with a switching matrix that allows device characterization through external test equipment [19]. A flow chart of a typical step-temperature experiment is shown in Fig. 1. At its heart, the device is stressed for some time at high power and at a set base-plate temperature, T_{stress}. After a certain stress time, we interrupt the stress, lower the base-plate temperature to 50 °C and characterize the device. We call this the "inner loop." After a number of

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http://dx.doi.org/10.1016/j.microrel.2014.09.019
0026-2714/

"inner loops" have been repeated, we detrap the device through an in-situ bake at 250 °C for 7.5 h, carry out a detailed characterization at 50 °C, increase to a higher T_{stress} and resume the high-power stress at this new base-plate temperature. We denote this the "outer loop." Through detailed experiments, we have determined that the 250 °C baking results in nearly complete device detrapping without introducing any significant degradation. This allows us to evaluate permanent device degradation, free of carrier trapping effects. Other detrapping methods commonly used such as visible or UV light illumination [20,21], are not available as these are packaged devices.

In our study, we focused on the degradation of the maximum drain current, I_{Dmax} (defined at V_{DS} = 5 V, V_{GS} = 2 V), and the drain resistance, R_D (defined as the extrinsic resistance on the drain side measured at 20 mA/mm using the gate current injection technique [22]). These figures of merit have been found to correlate most closely with RF power degradation [19,23,24]. Other figures of merit, such as R_S and I_{Goff} are also tracked. R_S is defined as the extrinsic resistance on the source side measured at 20 mA/mm using the gate current injection technique. I_{Goff} is defined as the gate current at V_{DS} = 0.1 V and V_{GS} = −5 V. We have verified that repeated measurement of these figures of merit under the selected conditions is "benign" and produces minimum changes in the device characteristics.

Device thermal models provided by the manufacturer in combination with an assessment of the electrical power supplied to the device are used to estimate the channel temperature during stress, $T_{channel}$.

3. Results

Typical results are shown in Fig. 2. Here, the device is stressed at V_{DSQ} = 40 V, I_{DQ} = 100 mA/mm with T_{stress} increasing from 50 °C to 230 °C for various lengths of time. We observe that the off-state gate current I_{Goff} increases by about 3 orders of magnitude starting at T_{stress} = 170 °C and saturating at T_{stress} = 190 °C (Fig. 2a) [10,12]. The maximum drain current I_{Dmax} starts to decrease at T_{stress} = 190 °C. By the time the device blows up at T_{stress} = 230 °C ($T_{channel}$ = 330 °C), I_{Dmax} has decreased by about 80%. R_D follows a degradation pattern that tracks that of I_{Dmax} (Fig. 2b). R_S exhibits much less degradation, as is commonly observed [25].

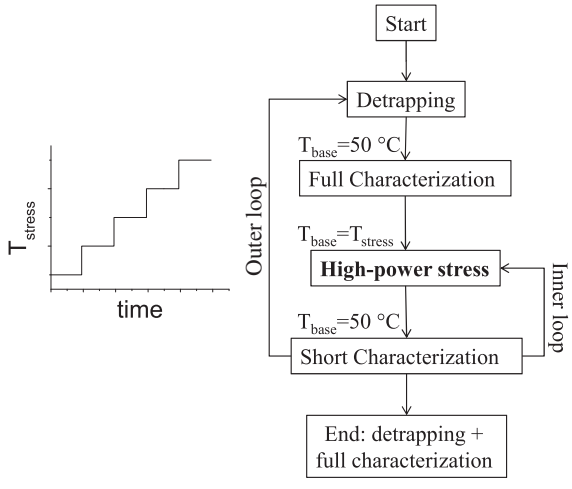

Fig. 1. Left: schematic of temperature evolution of the step-temperature stress experiments performed in this study. Right: flow chart of a typical experiment. A detrapping step brings the device to a reproducible detrapped state to assess permanent degradation. The device is stressed for a length of time and regularly characterized in an "inner loop". The stress temperature is stepped up periodically as the experiment flow goes through the "outer loop".

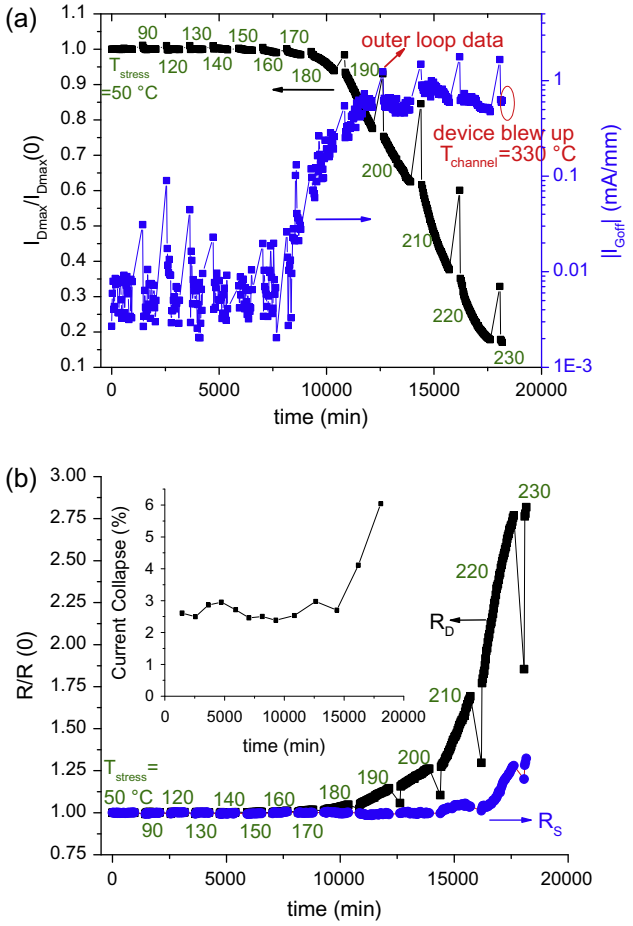

Fig. 2. Evolution of degradation of (a) normalized I_{Dmax} (defined @ V_{DS} = 5 V, V_{GS} = 2 V) and $|I_{Goff}|$ (defined @ V_{DS} = 0.1 V, V_{GS} = −5 V), (b) normalized R_D and R_S. Both outer loop and inner loop data are included in the graphs. Inset: current collapse measurements in the outer loop. The device was stressed at V_{DSQ} = 40 V and I_{DQ} = 100 mA/mm at a base temperature that increases from 50 °C up to 230 °C.

There is a marked difference between inner loop data (most of the data points) and outer loop data (those sticking out between different stress temperature steps) which are measured with the device freshly detrapped. Outer loop data reflects permanent damage while inner loop data also includes the effect of trapping. The difference between these two sets of data dramatically illustrates the impact of trapping. As is well known, electron trapping produced by high-voltage stress results in a reduction in the drain current of a HEMT due to a lowering of the sheet carrier concentration in the extrinsic drain close to the gate. Less known is the fact that electron trapping also reduces the HEMT gate current as the electric field at the edge of the gate is mitigated [21]. The data of Fig. 2 is consistent with a device that suffers considerable trapping in the inner loop but is detrapped in the outer loop.

Evidence of trapping can also be seen from in-situ current collapse measurements that we perform in the outer loop immediately after device detrapping (inset of Fig. 2b). Current collapse in GaN HEMTs is a temporary reduction of drain current immediately after the application of high voltage [26–28]. A conventional technique to assess current collapse relies on short-pulse characterization of the device. Here, we have adopted a relatively long pulse technique which can be carried out in standard DC characterization equipment and is amenable to integration with long-term stress experiments [29]. In this technique, with a device freshly detrapped and under V_{DS} = 0 conditions, a pulse of −10 V is applied to the gate for 1 s. This often triggers enough electron trapping for