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Investigation of high performance Edge Lifted Capacitors reliability for GaAs and GaN MMIC technology

Ming-Hung Weng [a,b,*], Chao-Hung Chen [a], Che-Kai Lin [a], Shih-Hui Huang [a], Jhih-Han Du [a], Sheng-Wen Peng [a], Walter Wohlmuth [a], Frank Yung-Shi Chou [a], Chang-Hwang Hua [a]

[a] WIN Semiconductors Corp., No. 35, Technology 7th Road, Hwaya Technology Park, Kuei Shan Hsiang, Tao Yuan Shien 333, Taiwan
[b] Current address: School of Electrical and Electronic Engineering, Newcastle University, Newcastle, NE1 7RU, UK

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ABSTRACT

This paper reports extensive investigations of Edge Lifted Capacitors (ELC) and standard metal–insulator–metal (MIM) capacitors with different refractive index and thickness of Silicon Nitride (Si_3N_4) dielectric films. The wafer-level electrical measurements reveal size dependence of capacitances and breakdown voltages. Physical characterization was performed using Fourier transform infrared spectroscopy (FTIR) to understand intrinsic properties of the studied films and failure-related cross sections were used to predict possible leakage mechanisms. Reliability testing of Human Body Model (HBM) and Machine Model (MM) electrostatic discharge (ESD), time-dependent dielectric breakdown (TDDB), and biased high temperature accelerated stress testing (bHAST) were performed and will be reviewed for GaAs and GaN monolithic microwave integrated circuit (MMIC) applications.

1. Introduction

In recent years, foundry services for GaN HEMTs on SiC devices [1–4] have gained remarkable attention due to the device's potential to revolutionize power and radio frequency (RF) electronics with predictions that the overall commercial and military markets will be multi-billion dollar markets by 2020 [5]. The move to high efficiency, low power consumption RF amplifier building blocks is seen to increase the GaN-based component demand. Since GaN HEMTs are operated at high voltage, passive components such as capacitors are also required to tolerate high voltages during circuit operation. GaN RF transistors typically operate at 28 to 50V and subsequently require capacitors, within the circuit, to withstand blocking voltages of > 200 V without damage [6–9]. The Silicon Nitride (Si_3N_4) dielectric film can be optimized by changing the Si_3N_4 composition and film stress using multi-layer plasma-enhanced chemical vapour deposition (PECVD) processes. The breakdown voltage is highly correlated to the electric field intensity within the capacitor dielectric. Therefore, a new Metal Insulator Metal (MIM) capacitor structure termed the Edge Lifted Capacitor (ELC) was developed. The high electric field around the capacitor periphery is effectively relieved in the ELC and thus the breakdown performance is significantly enhanced.

2. Devices structure and experiments

Capacitor fabrication starts with Metal1 as the bottom metal layer and Metal2 as the contact metal layer as shown in Fig. 1. A SPAN layer is formed to provide mechanical and structural support for the air bridge to minimize the parasitic capacitance. The overlay distance between SPAN and Metal1 creates desirable lifted metal edges of Metal2. In order to achieve high breakdown (V_{BD}) and simultaneously have high specific capacitance (C_P), the use of different capacitor arrays, ranging from 200 to 3.5×10^5 μm^2, and various Si_3N_4 stoichiometric film properties with refractive index (R.I.), ranging from 1.9 to 2.1, were used and compared. 123 different sites were characterized for each 100 mm wafer. Table 1 shows a summary of Si_3N_4 thickness and refractive index used in the experiments.

A total of five Si_3N_4 films have been studied with a 150 nm thick dielectric film used for Film_1 to Film_3 and a 300 nm thick dielectric film used for Film_4 and Film_5. The reference films, the process of record (POR) films, were also compared in this study. The difference in material properties of SiC substrates, such as transparency and higher thermal conductivity (300 W m^{-1} K^{-1} in SiC)

* Corresponding author.

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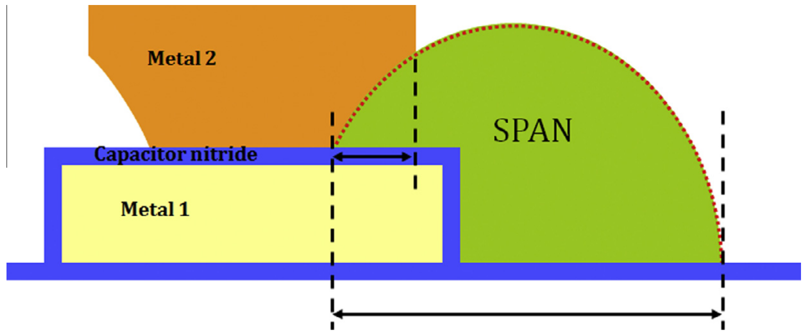

Fig. 1. Schematic cross section of an Edge Lifted Capacitor (ELC).

Table 1
Summary table of Si_3N_4 thickness and refractive index.

Film	Thickness (nm)	R.I.
1	150	2.1
2	150	2.0
3	150	1.9
4	300	2.0
5	300	1.9
Ref. POR1	150	1.95
Ref. POR2	150	2.0

as compared to GaAs substrates requires optimization of the Si_3N_4 film growth conditions. The flow rate, power, pressure and NH_3:SiH_4 ratio in the deposition process was varied resulting in different Si–N bond density and dielectric film refractive index. The bonding configurations within the film were examined by Fourier Transform Infrared Spectroscopy (FTIR). Before deposition of the Si_3N_4 film for the capacitor, a 200 nm thick Si_3N_4 film was deposited over the whole wafer isolating the substrate from the capacitor preventing leakage paths from contact pads to the substrate. Wafer-level electrical tests were performed using an Agilent 4072 high power supply with a Precio Octo auto prober. A voltage and current compliance of 200 V and 100 μA, respectively, is used to prevent probe melt-down. The intrinsic and extrinsic breakdown mechanisms are also characterized and fit to the Frenkel–Poole equation. The reliability performance testing included: human-body-model (HBM) and machine-model (MM) electrostatic discharge (ESD) [10], time-dependent dielectric breakdown (TDDB) [11], and biased high temperature accelerated stress (bHAST) [12] following JEDEC standards and guidelines to verify the reliability of the ELC capacitors. Finally, the capacitor geometry scaling is modelled using Advanced Design System (ADS).

3. Measurement results and discussion

Fig. 2 shows cross-sectional comparisons of the conventional MIM and the ELC designs. The conventional MIM design features a metal skirt which unintentionally results in a leakage path due to possible metal migration and concentrated electrical field. The ELC, on the other hand, provides a more robust capacitor, better leakage uniformity, and a 10 to 20% enhancement in the leakage behavior. This advantage is observed in the electrical characterization comparison between the MIM capacitors and the ELC with 1500 Å thick silicon nitride layers are manufactured with the SiH4/NH3 gas ratio (R = 0.65) and R.I. = 2 as shown in Fig. 3. These capacitors electrical characterization summarizes the leakage at the compliance current of 100 μA. As can be seen, the weak leakage

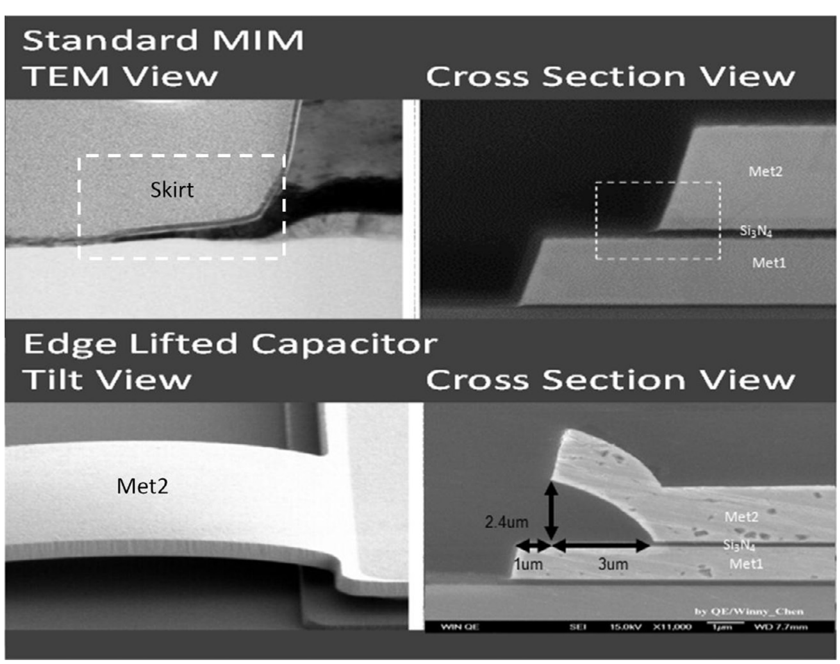

Fig. 2. SEM cross-section and side views of the ELC and MIM capacitors.