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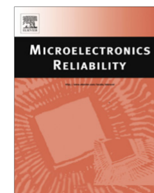

# Influence of the surface roughness of the bottom electrode on the resistive-switching characteristics of $Al/Al_2O_3/Al$ and $Al/Al_2O_3/W$ structures fabricated on glass at 300 °C

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ABSTRACT

Resistive-switching devices based on Metal–Insulator–Metal (MIM) structures have shown promising memory performance characteristics while enabling higher density of integration. Usually, these MIM devices are fabricated using different processing conditions including high temperature thermal treatments that could lead to undesirable chemical reactions in the insulator material and at its interface with the metals involved. In this work, we compare the electrical characteristics of MIM devices (fabricated on glass at 300 °C) that use aluminum or tungsten as bottom electrode (BE) in order to study the influence of a highly reactive (aluminum) or inert (tungsten) metal electrode on the memory characteristics. We found that the switching characteristics of $Al_2O_3$ (from a high-resistance state HRS to a low-resistance state LRS and vice versa), are highly dependent on the surface roughness of the BE, the thickness of $Al_2O_3$ and the current compliance (CC) which limits the electron density flowing through both top/bottom electrodes.

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## 1. Introduction

Recently, highly integrated MIM structures have shown the ability to switch between two different conduction modes in their insulators (whether metal oxides or solid electrolytes) by promoting formation/rupture of conductive filaments and/or ion migration between both electrodes after applying a potential difference in them [1–4]. This phenomenon of resistive switching is known as the *memristance* (memory resistance) effect [5,6] and the structures able to replicate it are known as Resistive Random-Access-Memory (ReRAM) devices. The memristance effect is defined as the ability to change the resistance state of a thin dielectric or solid electrolyte material from a usually high resistance state (HRS/OFF), to a low resistance state (LRS/ON) and vice versa; thus developing characteristic gate current–gate voltage (*Ig*–*Vg*) hysteresis loops. By properly controlling the resistive switching characteristics of many MIM structures, they have the potential to replace standard non-volatile memory technologies with higher performance characteristics (faster writing/erasing speeds, long data retention times, better endurance and ultra-low power consumption) along with a simple MIM architecture able to produce highly dense memory arrays.

For ReRAM operation, there are two characteristic switching modes: unipolar switching, which means the resistive switching depends on the amplitude of the applied voltage but not on the polarity; and bipolar switching, which means the resistive switching relies on the polarity of the applied voltage [7,8]. During switching, the HRS and LRS can be obtained by applying $V_{RESET}$ and $V_{SET}$ voltage pulses respectively. Importantly, an initial $V_{FORM}$ pulse is required to initiate the memory operation (forming the initial LRS) and usually, $V_{FORM} > V_{SET} > V_{RESET}$. Once these MIM devices reach the LRS, it is important to set up a limit on the current flowing through these devices since a large current density could damage the device permanently (the memristance effect will be lost). Usually, two different current limits are set up for the unipolar switching mode in which the formation of conductive filaments in the oxide (LRS, promoted by $V_{SET}$) is limited by a low current compliance in the measurement system, $CC_{SET}$. Dissolution of these conductive filaments in the oxide (HRS, promoted by $V_{RESET}$) is enhanced by setting a high current compliance, $CC_{RESET}$. In general, the correct setting of these electrical parameters ($V_{FORM} > V_{SET} > V_{RESET}$ and $CC_{RESET} > CC_{SET}$) enables a successful and reproducible operation of ReRAM devices based on MIM structures.

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On the other hand, even though the precise physics behind the ReRAM operation mechanism is still not fully understood, some observations [9–10] suggest that specific physical/chemical conditions of the electrodes/oxides play important roles for predictable resistive switching. This is important since we could use highly reactive or highly inert metal electrodes (having variable metal work functions) along with oxides having specific thermodynamic stabilities, band gap energies and therefore, different band-offsets to the metal electrodes (combined all-together, they would produce different conduction mechanisms prior to switching to a LRS).

In an effort to better understand the switching phenomena of ReRAM devices based on $Al_2O_3$, we present and compare the electrical, electronic and morphologic characteristics of MIM devices based on $Al/Al_2O_3/Al$ and $Al/Al_2O_3/W$ stacked structures deposited on glass and processed at 300 °C in order to assess their introduction into Back-End-Of-Line (BEOL) processing. By varying some parameters during the MIM fabrication process (different evaporation rates for the metallic BE and variable $Al_2O_3$ thickness), and by using different current compliances (*CC*) during memory operation, distinctive cyclic *I–V* characteristics can be correlated to those variations in the fabrication process which in turn, produce different carrier conduction mechanisms just before the initial switching to the LRS occurs.

## 2. Experimental

The sequential deposition of $Al/Al_2O_3/Al$ and $Al/Al_2O_3/W$ stacked structures were done on cleaned glass slides (Corning, 2947). These glass substrates have in average, a surface roughness of 1.26 nm (after AFM measurements in areas of 10 μm × 10 μm), ideal for sequential deposition of stacked materials. Since the most important regions of these MIM devices are the interfaces of its gate oxide with the metal electrodes (BE and TE), the good surface quality of a silicon substrate is not used at all. The aluminum or tungsten layers (used as BE) are 500 and 400 nm in thickness respectively, and they are used in two different MIM structures. The $Al_2O_3$ is 10 nm in thickness and is deposited by atomic-layer deposition (ALD) at 250 °C. After lithography (for gate pattern definition), the whole stack was annealed in $N_2$ at 300 °C.

For the initial cleaning procedure, the glass slides were degreased by sequential immersion in trichloroethylene (TCE) and acetone by 10/10 min, respectively, within an ultrasonic vibrator. Then, the slides were rinsed in deionized water (DI) by 10 min, and gently dried using an ultra-high purity $N_2$ pistol blow. Aluminum and tungsten were the first metal layers being deposited on already cleaned glass slides and they were used as bottom electrodes in two different MIM devices. These aluminum and tungsten layers were 500 and 400 nm in thickness and they were deposited by E-beam evaporation (Temescal BJD-1800 from Edwards) under ultra-high vacuum conditions using a deposition rate of 1 Å/s for both electrodes. After BE deposition, 10 nm of $Al_2O_3$ was deposited directly on these metals by ALD (Savannah-S100, from Cambridge Nanotech) at 250 °C using $H_2O$ and Trimethyl-Aluminum (TMA) as chemical precursors. During $Al_2O_3$ deposition, the ALD chamber was kept at 250 °C/200 m Torr of temperature/pressure for all 100 deposition cycles. Right after ALD of $Al_2O_3$, all samples were immediately moved back to the e-beam evaporator and the evaporation chamber was vacuumed down to $4 \times 10^{-7}$ Torr in order to minimize the exposure time of the $Al_2O_3$ surfaces to oxygen present in the atmosphere of the clean room. After reaching proper vacuum conditions, a relatively thick aluminum film ∼500 nm was then evaporated on top of $Al_2O_3$ with an evaporation rate of 1–2 Å/s. Aluminum was the last metal layer being deposited on $Al_2O_3$ and it was used as top electrode (TE) for both MIM devices. Once fully metalized, all samples were covered with positive photoresist using standard spinning/baking conditions and exposed to an UV system (Karl Suss MA6) to define the gate patterns of the MIM structures. A gate capacitor area of $64 \times 10^{-6}$ cm$^2$ was used for all MIM devices under test. After photolithography process, the final $Al/Al_2O_3/Al$/Glass and $Al/Al_2O_3/W$/Glass stacks were annealed in pure $N_2$ (99.999% purity) at 300 °C in order to promote densification of the gate oxide and its interfaces with both metal electrodes. As noticed, the fabrication procedure is quite simple while the maximum processing temperature is 300 °C, ideal for integration into BEOL processing. Fig. 1 shows the complete fabrication processing flow for the MIM structures along with a simplified MIM's schematic and memory array.

On the other hand, the surface roughness for the first metal layer (aluminum or tungsten as BE) was measured by atomic-force microscopy (AFM by NanoSurf EasyScan-2) and by taking into account 10 different spots for three samples having similar deposition conditions. Finally, capacitance–voltage (*C–V*, 1 kHz – 3 MHz) and current–voltage (*I–V*) measurements were both obtained using a Semiconductor Device Analyzer (SDA, B1500A from Agilent), and by taking into account 10 different samples for each measurement condition. All electrical measurements were obtained at room temperature.

## 3. Results and discussion

### 3.1. Electrical characteristics of MISCAP using $Al_2O_3$ as gate oxide

First of all, and in order to obtain the electrical quality of the proposed insulator, it is important to test the electrical characteristics of only the $Al_2O_3$ used in both MIM devices. For this, we deposited a thinner $Al_2O_3$ layer (6 nm in thickness, using the same ALD and annealing conditions) directly on hydrogen-terminated *n*-type silicon and measured several Metal–Insulator–Semiconductor capacitors (MISCAP). Fig. 2 shows the gate current vs. gate voltage characteristics (*Ig–Vg* under accumulation, before and after hard-breakdown), of 10 different MISCAP ($Al/Al_2O_3$/n-Si) until the ultra-thin gate oxides reach breakdown. We notice a high uniformity in the *I–V* characteristics (including almost the same breakdown voltage) because of the high quality of the ALD technique that produces excellent uniformity in the oxide thickness even at the atomic level [11,12]. For MIM structures, any deviation from these ideal *I–V* characteristics could then be related to the metals used as BE.

### 3.2. Bipolar resistive switching in $Al/Al_2O_3/Al$ and $Al/Al_2O_3/W$ structures

Fig. 3(a) shows the resistive switching characteristics of the $Al/Al_2O_3$/Al-MIM structure in semilog format. Each electrical test for the same MIM device consists of applying a double sweep of voltage. These initial *I–V* characteristics are similar to that of bipolar switching. The first sweep (negative polarity, from −5 V down to 0 V) shows that the memory device is initially in the LRS (ON, reaching the CC) and when the voltage is reduced in magnitude, the device then switches to the HRS. For the positive polarity, the device shows an opposite conduction behavior. Now, when the voltage sweeps back to −5 V (to complete one full sweep cycle), the device is kept in the LRS (OFF). For a new full sweep cycle, the whole behavior is also observed although the $V_{SET}$ is now reduced. Here, $V_{FORM} > V_{SET}$ as expected, while the $I_{OFF}/I_{ON}$ ratio is around 6 orders of magnitude, which is a large resistivity window and quite useful in order to obtain long lasting and large endurance cycles during memory performance. In this case, the *N*th cycle refers to the 8th *I–V* sweep and we notice that the gate current before $V_{SET}$ is kept lower compared to its original level (positive

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