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A yield improvement technique in severe process, voltage, and temperature variations and extreme voltage scaling

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ABSTRACT

Drastic yield reduction at sub/nearthreshold voltage domains, caused by the severe process, voltage, and temperature (PVT) variations in this region, is challenging characteristic of recent nanometre sensory chips. Using a variation sensitive and ultra-low-power design, this paper proposes a novel technique capable of sensing and responding to PVT variations by providing an appropriate forward body bias (FBB) so that the delay variations and timing yield of whole system as well as energy-delay product (EDP) are improved. Theoretical analysis for the error probability, confirmed by post-layout HSPICE simulations for an 8-bit Kogge–Stone adder and also two large Fast Fourier Transform (FFT) processors, shows considerable improvements in severe PVT variations and extreme voltage scaling. For this adder, for example, the proposed technique can reduce error rate from 50% to 1% at 0.4 V. In another implementation, in average ~7× delay variation and ~4× EDP improvement is gained after this technique is applied to an iterative 1024pt, radix 4, complex FFT while working in sub/nearthreshold voltage region of 0.3 V–0.6 V. Also, pipelined version of the FFT consumed only 412pJ/FFT at 0.4 V while processing 125 K FFT/sec.

1. Introduction

With the introduction of 65 nm technologies, reliability of circuits started to challenge the transistor scaling which is an essential trend for continuation of performance, area and energy improvements in silicon chips fabricated for sensory systems.

Increasing defects in fabrication process as a result of aggressive transistor scaling is the source of this unreliability which reduces manufacturing yield. As it will be seen, the final yield for ultra-low power circuits depends on reliability (or resilience to temperature variation and voltage noise) and satisfying the performance and energy goals which are all correlated, and if not met, the specific die will be discarded. These challenges are pronounced even more seriously at the subthreshold voltages, from which low energy wireless applications benefit the most by trying to minimize the power use for a given performance requirement [1]. As PVT variations rise exponentially with the voltage scaling, this results in a dramatic uncertainty and still urges designers to employ adaptive body-bias (ABB) techniques [2] despite the fact that technology scaling counteracts the body biasing effect (with the increase of dopants in the below 100 nm device channels to cause stronger inversion).

Although efficient in the superthreshold region, the impact of the body biasing is especially sensed at the subthreshold voltages because of the exponential increase in the sensitivity of devices to the threshold voltage. For example in a typical 90 nm technology, if threshold voltage is changed by 50 mV at a 1 V supply voltage, delay varies 13% whereas it results in a 55% delay increase at a 0.45 V supply voltage [3].

As mentioned, susceptibility to noise or voltage variations is a major source of performance failure at subthreshold voltages. Because threshold voltage (V_{TH}) is managed by an independent doping process, V_{TH} in PMOS and NMOS devices can be different considerably. This, for example, can result in an insufficient high output voltage at the fast NMOS slow PMOS corner (in which NMOS devices are much leakier than PMOS ones) or an insufficient low output voltage at a fast PMOS slow NMOS corner. Consequently, not only noise margins can be violated at process corners, but also either rising or falling time is extremely long which in return results in increased timing breaches.

As PMOS and NMOS transistors can be controlled independently using body biasing techniques, this opens many opportunities for designers to optimally tune the β-ratio and preventing V_{TH} mismatch problems. For example, authors in [4] used V_{TH} balancing

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schemes which enabled them to implement a supply voltage scaling from superthreshold to subthreshold voltages. Their body biasing technique adapts P/N-ratio dynamically while voltage scaling.

Authors in [5] also studied the capability of ABB techniques to address these variations and implemented a sub-threshold processor to show its effectiveness. They also proved that a body bias which optimises β-ratio for noise margin also minimises energy per instruction [6].

In this paper, the purpose is addressing the challenge of timing yield reduction at subthreshold voltages. An extreme process variation sensitive and ultra-low power (SULP) FBB circuit is proposed capable of addressing PVT variations, while V_{DD} is scaling, by tuning β-ratio in different process corners. This technique helps improve the system performance and hence timing yield by applying FBB to NMOS and/or PMOS networks at lower voltages and/or lower temperatures and applying appropriate FBB to slower devices depending on the process variation.

In addition to sensing the PVT variations, the proposed technique is at the same time capable of reacting to the voltage level under which the circuit is working. This means that if a circuit has a low voltage level or any other performance restricting conditions (due to PVT variations), the proposed technique detects it and helps the system cope with the PVT variations which are more pronounced at low voltages. The originality of this technique is in its capability to handle harsh temperature and process variations while addressing aggressive voltage scaling that is unprecedented in the literature.

On the other hand, this extra help is withdrawn when the system is working in high voltage levels or any other high performance circumstances. This results in considerable reduction of functionality failures at slow conditions and no energy overhead at fast situations which adds to the technique's originality as well. This technique also leads to a significant improvement in production yield as a result of its adaptive approach towards PVT variations as well as voltage reductions.

Another factor important to timing yield is delay variation which is enormously improved by this technique as it will be seen. Simplicity of the design and also its low power operation incurs low energy and negligible area overhead to the static CMOS system this FBB has been applied to. Results prove that the exponential sensitivity of devices to variations in subthreshold voltages can still be exploited to an extent that can compensate the diminishing FBB effectiveness caused by technology scaling. By scaling voltage form 0.8 V to 0.3 V and temperature changes of −15 °C to 75 °C, error probability in the simulated 8-bit Kogge–Stone adder was decreased from 50% to 1% at 0.4 V as a result of this technique.

The outcome of mixed signal simulations on a 1024 point, radix 4, 32 × 32bit complex input iterative FFT processor showed not only seven times improvement in delay variations, but EDP was also reduced to around 4 times, after this technique was applied, which showed the real benefit of the technique lying in large scale circuits.

Finally, a pipelined version of the FFT consumed 412pJ/FFT which was ∼43 times less than the latest sub/nearthreshold FFT processor while being only ∼1.9 times slower (with 125 K FFT/sec throughput). SULP FBB also resulted in ∼250% delay improvement in this pipelined FFT processor, with respect to a ZBB FFT processor, with 34% energy overhead.

The demonstrated mathematical platform also helps designers understand and adjust the parameters and factors which have the highest and lowest sensitivity in the output of a particular sub/nearthreshold circuit. They can also analyse and predict, with a high accuracy, what effects a technique can have on a design under test, and optimise the approach mathematically.

The rest of this paper describes how SULP FBB circuit can achieve this by firstly mathematically analysing how circuit works and why it reduces error rate in Section 2, and then, in Section 3, providing the HSPICE simulation results obtained from post-layout Monte Carlo runs to back the theoretical findings.

2. Objective, functionality and theoretical analysis of the proposed circuit

2.1. Objective

Fig. 1 shows the schematic of the proposed SULP FBB generator introduced in [7] which was used to apply FBB to the MOS devices so that the EDP of system was improved and process, voltage and temperature (PVT) variations were addressed while system was working in subthreshold voltages. The main duty of the SULP FBB technique was to address inter-die process variations by applying the appropriate FBB to the whole system.

It should be noted that inter-die and intra-die process variations are considered independent parameters and their effects are usually represented by different uncorrelated random variables [8]. As the SULP FBB technique has been characterised and confirmed, in this paper, for tackling inter-die process (as well as temperature and voltage) variations, the final results on the improvement of performance, power and reliability will be independent of intra-die process variations. That is, final results will even enhance, should this (or any other) technique be used for handling intra-die and random process variations. In a 22 nm technology, for example, the issue of inter-die variation will still be present, even worse than before, and the proposed technique will still be applicable for such technologies. Nevertheless, a 22 nm circuit with the proposed technique applied to, will still benefit from other techniques to compensate intra-die and random variations which may not be addressed by the proposed circuit.

It is worth mentioning that this technique has a very small area overhead by having the total area of 168.7 μm^2. Besides, this small

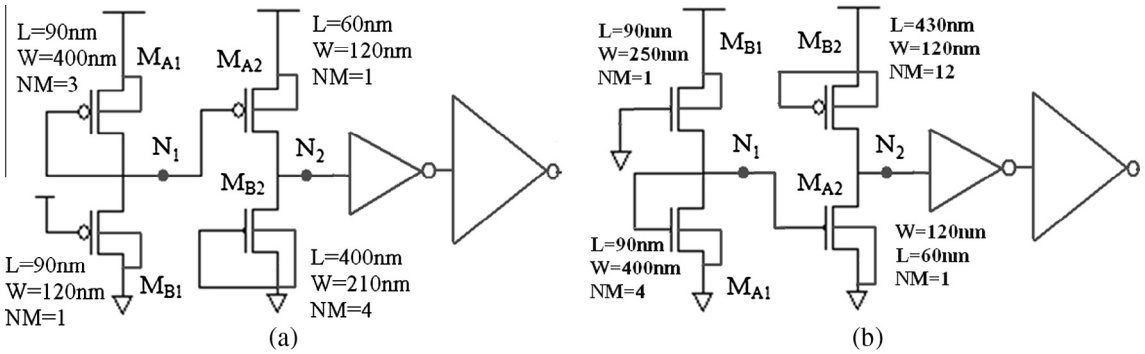

Fig. 1. Body Bias generators for a) PMOS network and b) NMOS network.

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