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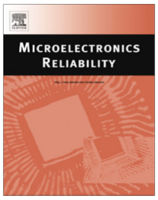

Mechanical and electrical properties of ultra-thin chips and flexible electronics assemblies during bending

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ABSTRACT

Ultra-thin chips of less than 20 μm become flexible, allowing integration of silicon IC technology with highly flexible electronics such as food packaging sensor systems or healthcare and sport monitoring tags as wearable patches or even directly in clothing textile. The ultra-thin chips in these products will be bent to a very high curvature, which puts a large strain on the chips during use.

In this paper a modified four-point bending method is presented, which is capable of measuring chip stress at high curvatures. The strength of several types of ultra-thin chips is evaluated, including stand-alone ultra-thin test chips and back-thinned 20 μm thick microcontrollers, as well as assemblies containing integrated ultra-thin microcontroller chips. The effect of chip thickness, bending direction and backside finish on strength and minimum bending radius is investigated using the modified four point bending method. The effect of bonding ultra-thin chips to flexible foils on the assembly strength and minimum bending radius is evaluated as well as the effect of bending on electrical properties of the bonded microcontroller dies.

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1. Introduction

Large area systems in foil (SiF) often consist of integrated thin components which are assembled on a flexible substrate. Typical elements include data processing chips, wireless communication chips, autonomous power (battery, solar cell) or a display and sensors, all of which are distributed over a large area on very thin or stretchable polymer film substrates [1,2]. Application examples of these flexible, ultrathin and low-cost packages include monitoring sensors attached to food packaging, smart bandages that monitor the healing of wounds and smart active RFID tags [3,4]. Thin, flexible electronics can even be integrated in smart textiles for (sports-) clothing [5]. Silicon IC chips are often added for high performance functionality of the flexible microsystem [6]. Preferably, the IC chips are integrated in a thinned, bare die form so the flexibility of the foil based assembly is not compromised [7–9]. Besides the electronic performance, the thin bare die chips for these systems must have good mechanical strength [10].

Therefore, the experimental validation of the mechanical strength of ultra-thin chips is essential for determining the resilience of the complete flexible system. Well known chip testing methods include ball-on-ring, three- and four-point bending and flex testing. Of these methods, ball-on-ring generally overestimates the strength of the chips in the flexible system. The ball-on-ring test is useful for determining the volume strength of the material because the maximum stress is only achieved at the center of the die [7], therefore neglecting edge damage effects. Edge damage effects are however an important cause of failure [11], especially in chips in flexible electronics assemblies, because the whole chip including the edges will be bent when the system is deformed. In three-point bending tests edge damage is taken into account since the edges do experience stress [11]. However, three-point bending on average also overestimates the chip strength [12], unless the exact crack position can be measured. The maximum stress is only achieved at the midpoint of the die and the correct fracture strength of the chip can only be calculated correctly if the crack initiation position is known [13]. This is especially important when testing functional chips with features that are distributed non-uniformly across the die. In addition the three-point bending strength is dependent on the distance between the supports [15], induces shear stresses in the sample and also suffers from non-linear effects at high deformations [14,16,17]. These include effects that originate from horizontal

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forces at the supports resulting and mechanical tolerances of the set-up. Hence these two methods are less suitable in predicting strength of thin chips realistically for flexible electronics applications. Four-point bending is a very suitable technique for brittle materials, because the stress between the inner supports is uniaxial and constant [13,15]. However, conventional four-point bending techniques also suffer from the aforementioned non-linear effects for large deformations [14,18]. Certain precautions are needed when applying four-point bending methods to characterize the fracture stress of ultra-thin chips bent to a high curvature, as will be explained in this paper. We therefore have devised a four-point bending test setup suitable for testing ultra-thin chips at high curvature. The corresponding test method is based on monitoring the curvature of the chip during bending and determining the stress from the measured curvature. The setup is used to characterize the mechanical strength of several types of chips, blank silicon dies, dummy test chips and fully functional microcontroller ICs. In addition to mechanical strength of the stand-alone chips, the mechanical strength of assemblies of ultra-thin chips on foil is important for applications in flexible and conformable electronics. In addition to the influence of bonding stresses on the minimum bending radius, the flexible thin assemblies the chips will be bent to a low radius and the layers of the assembly located outside the neutral plane will experience increased bending stresses. Several studies have shown that the piezoresistivity of silicon will have effects on the functionality of the ICs [7,19–22]. In this paper the influence of bending on the performance of functional ultra-thin flexible electronics assemblies is shown.

2. Four-point bending modeling

In Fig. 1, the principle of a four-point bending test is displayed. The lower supports move a distance d_z by applying force F on the test specimen while the upper supports are fixed. The thickness and material parameters of the specimen determine the amount of bending.

When bending thick chips up to failure, the curvature remains limited ($d_z \ll a$) and non-linear effects are negligible. Therefore the maximum stress in the chip can be calculated in a straightforward manner, using the conventional four-point bending approximations for low deflections [19]. The stress in the die is at a maximum in the region between the inner support struts. In this area, the stress is equal to:

$$\sigma = \frac{3Fa}{wt^2} \tag{1}$$

where F is the applied force, w is the width of the chip and t is the thickness of the chip and $a = L - L_i$ where L is the distance between the outer supports, L_i is the distance between the inner supports.

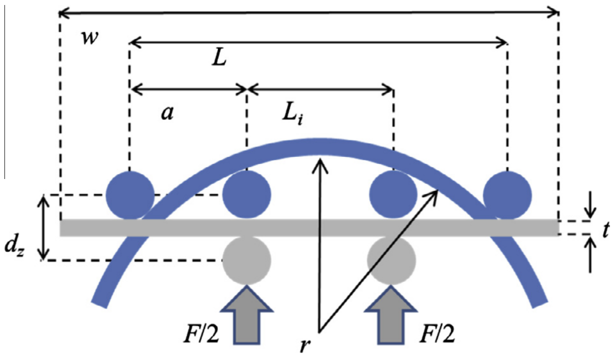

Fig. 1. Schematic of the four-point bending principle.

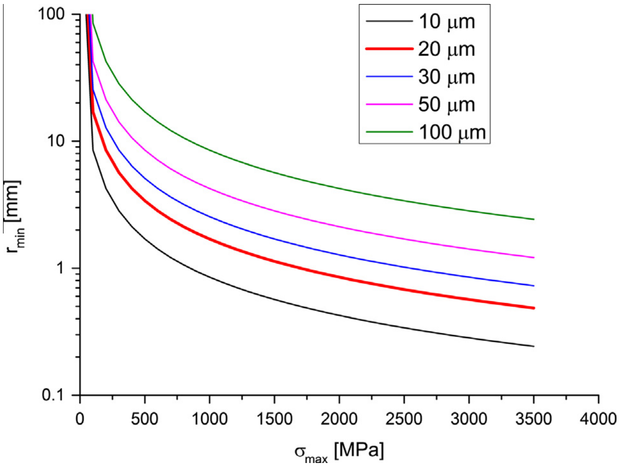

Fig. 2. Relation between die strength and minimum bending radius of stand-alone dies for different dies thickness.

The stress between the inner supports can also be estimated using the displacement of the supports as input [19]:

$$\sigma = \frac{-3d_zEt}{a(3L-4a)} \tag{2}$$

where d_z is the displacement of the supports in z-direction (i.e. perpendicular to the bending plane) and E is the elastic modulus of the die. As mentioned this linear approximation is only valid for deflections ($d_z \ll$ a) [18].

For thin chips, the curvature is high and non-linear effects cannot be neglected. The stress at high curvature is calculated from the radius of the chip. The radius, r, can derived from the chip curvature (see Fig. 1). The bending stress along the cross section of the die can be calculated from the radius of curvature. The curvature, κ, of a function $y = f(x)$ in Cartesian coordinates is equal to [18]:

$$\kappa = \frac{1}{r} = \frac{d^2y/dx^2}{\left(1+(dy/dx)^2\right)^{2/3}} \tag{3}$$

where r is the local bending radius.

The stress in the chip can be calculated from the radius of the chip using the following relation:

$$\sigma_x = \varepsilon_x E = \frac{y}{r}E \tag{4}$$

where σ_x and ε_x are the stress and strain in x-direction (see Fig. 3 for axes definitions) and y is the distance from the center of the chip.

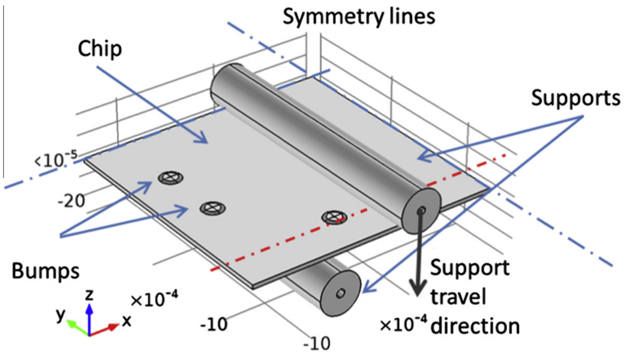

Fig. 3. Four-point bending model. For symmetry reasons ¼ of the structure is modeled. The black arrow points in the direction of the support travel. The bottom support is fixed. The red cut-line runs along the bottom of the chip under the middle of the bumps. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

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