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Reliability matrix solution to multiple mechanism prediction ☆

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ABSTRACT

We present a method for predicting the failure rate and thus the reliability of an electronic system by summing the failure rate of each known failure mechanism. We use a competing acceleration factor methodology by combining the physics of failure for each mechanism with its own effect as observed by High/Low temperature and High/Low voltage stresses. Our Multiple High Temperature Overstress Life-test (M-HTOL) method assumes that the lifetime of each failure mechanism follows constant rate distribution whereby each mechanism is independently accelerated by its own stress factors. Stresses include temperature, frequency, current, and other factors that can be entered into a reliability model. The overall failure rate thus, also follows an exponential distribution and is described as the standard FIT (Failure unIT or Failure in Time). This method combines mathematical models for known failure mechanism and solves them simultaneously for a multiplicity of accelerated life test results to find a consistent set of weighting factors for each mechanism. The result of solving the system of equations is a more accurate and a unique combination for each system model by proportional summation of each of the contributing failure mechanisms.

1. Background

Reliability device simulators have become an integral part of the VLSI design process. These simulators successfully model the most significant physical failure mechanisms in modern electronic devices, such as Time Dependent Dielectric Breakdown (TDDB), Negative Bias Temperature Instability (NBTI), Electromigration (EM) and Hot Carrier Injection (HCI). These mechanisms are modeled throughout the circuit design process so that the system will operate for a minimum expected useful life. Modern chips are composed of tens or hundreds of millions of transistors. Hence, chip level reliability prediction methods are mostly statistical. Chip level reliability prediction tools, today, model the failure probability of the chips at the end of life, when the known wearout mechanisms are expected to dominate. However, modern prediction tools do not predict the random, post burn-in, failure rate that would be seen in the field [1–4].

Chip and packaged system reliability is still measured by a Failure unIT, also defined as the Failure-In-Time (FIT). The FIT is a measure of the constant rate function (Poisson model) failure rate, λ. This model is time-independent, and the failure rate in FIT is defined as the number of expected device failures per billion part hours. A FIT is assigned for each component multiplied by the number of devices in a system for an approximation of the expected system reliability. The semiconductor industry provides an expected FIT for every product that is sold based on operation within the specified conditions of voltage, frequency, heat dissipation and etc. Hence, a system reliability model is a prediction of the expected mean time between failures (MTBF) for an entire system as the sum of the inverse FIT rate for every component.

A FIT is defined in terms of an acceleration factor, *AF*, as:

$$FIT = \frac{\#\text{failures}}{\#\text{tested} * \text{hours} * AF} \cdot 10^9 \quad (1)$$

where #failures and #tested are the number of actual failures that occurred as a fraction of the total number of units subjected to an accelerated test. The acceleration factor, *AF*, must be supplied by the foundry since only they know the failure mechanisms that are being accelerated in the final High Temperature Operating Life (HTOL) test. This factor is generally based on a company proprietary variant of the MIL-HDBK-217 approach for accelerated life testing. The true task of reliability modeling, therefore, is to choose an appropriate value for *AF* based on the physics of the dominant failure mechanisms that would occur in the field for the device.

The HTOL qualification test is usually performed as the final qualification step of a semiconductor manufacturing process. The

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test consists of stressing some number of parts, usually 77 (for example) [8], for an extended time, usually 1000 h, at an accelerated voltage and temperature. Two features shed doubt on the accuracy of this procedure. One feature is lack of sufficient statistical data and the second is that companies generally present zero-failure results for their qualification tests and hence stress their parts under relatively low stress levels to guarantee zero failures during qualification testing.

The current, industry accepted, standard approach for measuring FIT would be correct if there were only a single dominant failure mechanism that is excited equally by either voltage or temperature. Additionally, this same mechanism should be the only one that is accelerated by the burn-in or accelerated test. For example, electromigration is known to follow Black's equation and is accelerated by increased stress current in a wire or by increased temperature of the device. If, however, multiple failure mechanisms are responsible for device failures, each failure mechanism should be modeled as an individual "element" in the system and the component reliability is modeled as the survival probability of all the "elements" as a function of time.

This limitation has been recognized in the latest JEDEC standard, JEP-122G:

> *When multiple failure mechanisms and thus multiple acceleration factors are involved, then a proper summation technique, e.g., sum-of-the-failure rates method, is required* [5].

If multiple failure mechanisms, instead of a single mechanism, are assumed to be time-independent and independent of each other, the Failure unIT, FIT (assuming constant failure rate approximation) should be a reasonable approximation for realistic field failure rate, λ. Under the assumption of multiple failure mechanisms, that each will be accelerated differently depending on the physics that is responsible for each mechanism. If, however, an HTOL test is performed at an arbitrary voltage and temperature for acceleration based on a single failure mechanism, then only that mechanism will be accelerated. In most devices, hence, the reported FIT (especially one based on zero failures) will be meaningless with respect to other failure mechanisms.

2. Multiple failure mechanism model

Qualification for failure rate prediction has not improved over the years. Nonetheless, the semiconductor industry's understanding of reliability physics of semiconductor devices has advanced enormously. Every known failure mechanism is so well understood and the processes are so tightly controlled that electronic components are designed to perform with reasonable life and with *no single dominant failure mechanism*. Standard HTOL tests generally reveal multiple failure mechanisms during testing, which would suggest also that no single failure mechanism would dominate the FIT rate in the field. Therefore, In order to make a more accurate model for FIT, a preferable approximation should be that all failures are linearly *proportional* and the resulting overall failure distribution resembles a *constant failure rate process* that is consistent with the mil-handbook, FIT rate approach [6].

The acceleration of a single failure mechanism is a highly nonlinear function of temperature, voltage and/or current [1–6]. The temperature acceleration factor (AF_T) and voltage acceleration factor (AF_V) can be calculated separately and is the subject of most studies of reliability physics. The total acceleration factor of the different stress combinations will be the product of the acceleration factors of temperature and voltage,

$$AF = \frac{\lambda(T_2, V_2)}{\lambda(T_1, V_1)} = AF_T \cdot AF_V = \exp\left(\frac{E_a}{k}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)\right) \exp\left(\gamma_1 (V_1 - V_2)\right) \tag{2}$$

This acceleration factor model is widely used as the industry standard for device qualification. However, it only approximates only a single generic type of failure mechanism and does not correctly predict the acceleration of other mechanisms or combinations [5].

To be more correct, however, electronic devices should be considered as comprising several failure mechanisms that degrade simultaneously [5]. Each mechanism 'competes' with the others to cause an eventual failure. When more than one mechanism exists in a system, then the relative acceleration of each one must be defined and averaged at the applied condition. Every potential failure mechanism should be identified and its unique *AF* should then be calculated at a given temperature and voltage so that its FIT can be approximated separately from the other mechanisms. Then, the final FIT will be the sum of the failure rates per mechanism, as is described by:

$$FIT_{total} = FIT_1 + FIT_2 + \ldots + FIT_i, \tag{3}$$

such that each mechanism leads to an expected Failure unIT per mechanism, FIT_i.

Unfortunately, however, individual failure mechanisms are not uniformly accelerated by a standard HTOL test, and the manufacturer is forced to model a single acceleration factor that cannot be combined with the known physics of failure models [6]. Whereas each intrinsic mechanism is known to have different statistical distributions, the combination of distributions becomes, at the ensemble level, approximately constant rate as well known by Drenick [7]. This theorem justifies the summation of failure rate approach suggested here, also as explained in the JEDEC handbook [5].

3. Matrix approach

The basic method for solving the system of failure mechanism equations is described in the paper from Bernstein et al. [6]. In combination with the suggestion of a Sum-of-failure-rate method as described in JEDEC Standard JEP122G [5], a matrix should be able to combine the theoretical acceleration with measured device degradation. Also, the formulae for each mechanism are well studied and published. Thus the prediction of microelectronic system reliability (matrix approach) that follows logically is described here.

The matrix approach we present here, to model useful life failure rate (FIT) for components in electronic assemblies, begins by assuming that each component is composed of multiple failure mechanisms based on its operation, rather than simply a sum of sub-components. For example; Electromigration, Hot-Carrier, NBTI and TDDB are each seen as sub-components of the complete chip. We need to make the statistical assumption that each mechanism has its own acceleration factor related to voltage, temperature, frequency, cycles, etc. Each sub-component is assumed to approximate the relative likelihood of each mechanism as a proportion of the system FIT. Then, each component can be seen as a summation of intrinsic degradation by individual failure mechanisms multiplied by its relative proportion. Of course we know that statistically, each mechanism has its unique probability in time, however we invoke Drenick's theorem [7] again to allow the simultaneous solution, which will be more correct in the real world. We can, thus, use a matrix of mechanism models, each with it is own relative weight for that individual mechanism, assuming they are all constant-failure-rate processes. Hence, the standard system reliability FIT can be modeled using traditional MIL-handbook-217 type of algorithms and adapted to known system reliability tools.

This approach allows accelerated testing to be performed at increased voltages, temperature and power levels to increase the separation of individual mechanisms in order to calibrate this matrix to actual components in a system. The matrix is then solved