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Dopant transfer from poly-si thin films to c-Si: An alternative technique for device processing

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ABSTRACT

An alternative technique for production of devices which uses both silicon crystalline wafers (p-type) and heavy doped amorphous silicon thin films (n-type) is reported. The amorphous silicon acts as a finite source of dopant and is deposited (at low temperature, 70 °C) by plasma enhanced chemical vapor deposition on silicon wafers. Afterwards, the process of dopant diffusion into the crystalline silicon occurs in a diffusion furnace at 1000 °C for 2 h, to create p–n junctions. Using SIMS analyses, a dopant (P) transfer into c-Si of about 30% is verified and 87% of the dopant transferred is electrically active. Consequently, n-MOSFET devices are produced using a gate oxide thermally grown at the same diffusion temperature for one hour. The preliminary results of the MOSFET (channel length and width of 0.5 and 5 mm, respectively) show a depletion behavior with a threshold voltage, $V_{th} = -8.2$ V and afield-effect mobility, $\mu_{FE} = 187.8$ cm^2/(Vs).

1. Introduction

The development of microelectronic device technologies started in the 60s with an industrial implementation in the 70s. Nowadays, we are surrounded by equipment assembled with electronic devices. The fact that these devices are produced at an industrial level does not mean that the processes employed for their production may not be improved. The present work reports a new pre-deposition technique for the diffusion process of crystalline silicon doping, with the advantage of using less energy, when compared to the conventional production method [1]. Two of the processing stages that are usually executed at high temperatures (≈ 1000 °C) are eliminated – (1) the oxidation for mask purposes and (2) the thermal pre-deposition. The novelty consists in the pre-deposition of a highly doped amorphous silicon thin film that will act as a finite source of dopant of a known dose. The amorphous silicon film is deposited by plasma enhanced chemical vapor deposition (PECVD) at low substrate temperature (70 °C) [2,3]. Subsequently, a diffusion at 1000 °C for 2 h is made and the resulting junction is analysed. Next, n-type field effect transistors are fabricated. The MOSFET dimensions are: channel length and width of 0.5 and 5 mm, respectively. The main characteristics of n-MOSFETs achieved are reported.

2. Experimental

Two samples of p-type crystalline silicon (Cz, ⟨100⟩, $\rho = 1$–$20\ \Omega$ cm) with size 10×10 mm^2 are used as substrates for highly doped hydrogenated amorphous silicon (a-Si:H) thin films deposition. Sample A, with 3440 Å film thickness, will be used for determination of P concentration in a-Si:H by SIMS. A thickness higher than 3000 Å is needed for a better film analysis. Sample B, deposited with the same conditions of sample A but with 506 Å film thickness, will be used as a solid source of P for diffusion in c-Si (Table 1). This small thickness facilitates the a-Si:H dehydrogenation process.

These substrates, intended only for diffusion study purposes, are cleaned with anion free detergent and next rinsed with ultrapure water ($\rho = 18.2$ M Ω cm) to conclude the cleaning. The amorphous silicon films are deposited by PECVD (13.56 MHz) at 70 °C. The phosphine (PH_3) concentration used in the gas phase is 1.5% in silane, with a total flow of about 10 sccm. The film is deposited with a growth rate of 2.25 Å/s, until a final thickness of 500 Å is achieved. The other deposition parameters are reported in detail elsewhere [4]. The area of the amorphous film is defined using a lift-off lithography process: AZ1518 photoresist, 2 μm thick, is previously patterned leaving windows where junctions are to be made. Next, a-Si:H is deposited and then the photoresist is removed, leaving the a-Si:H patterned on the substrate. Samples

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Table 1
Characteristics of the samples used for SIMS measurements.

Sample	a-Si:H thickness(Å)	Processing
A	3440	As-deposited
B	506	After diffusion

are then placed in the tubular diffusion furnace at room temperature. The temperature is then quickly raised until 350 °C. From 350 °C to 550 °C a soft ramp is applied (0.8 °C/min), to avoid blistering phenomena [5,6]. In this range of temperatures, the a-Si:H dehydrogenation occurs. This step would not be necessary if the a-Si was deposited by other technique (e.g. sputtering), but the PECVD technique allows a much better control of P concentration. Finally, temperature rate is increased to 10 °C/min and kept constant until 1000 °C where the diffusion begins for 2 h. In the last 11 min of the diffusion process, a wet oxidation will occur simultaneously to diffusion on order to oxidize the deposited silicon. This oxide will be removed by wet etching, using a BHF solution.

For MOSFET production, RCA1 and RCA2 cleaning procedures are used in first place, followed by a-Si:H deposition, dehydrogenation and diffusion as mentioned above. Next, an oxide layer (SiO_2), 2190 Å thick, is grown at the same temperature by wet oxidation process for 1 h. After contact window lithography, the aluminum contacts, 1500 Å thick, are deposited by Thermal Evaporation. These contacts are then annealed at 450 °C for 30 min. The thickness measurements of the a-Si:H, oxide layer and aluminum films are made by Veeco Dektak III. The electrical characterization of the devices is made through I(V) curves (conductance or transconductance curves), using a Keithley 617 programmable electrometer and a Keithley 228A voltage/current source. Sheet resistance is measured by a Veeco FPP5000 four point probe. In depth chemical characterization is made by Probion (France) using a Secondary Ion Mass Spectrometry (SIMS) apparatus (see Table 2). A picture of the MOSFET produced is presented in Fig. 1a and the size of different regions in Fig. 1b.

3. Results and discussion

3.1. Efficiency of dopant transfer from pre-deposited layer to c-Si

SIMS analysis was performed in doped amorphous silicon thin films after deposition (Fig. 2), as well as in the crystalline silicon after diffusion (Fig. 3), in order to characterize the dopant concentration profile. Considering the dose (Q_{A0}) initially present in the thin-film, the fraction of dopant which has diffused from a-Si to c-Si can be calculated, using both SIMS profiles. On the other hand, the knowledge of the dose present in the c-Si allows to obtain the fraction of atoms which are electrically active, comparing the data from SIMS and from the four-point probe measurements. If all atoms were electrically active, the sheet resistance (R_S) would be

Table 2
Details of SIMS measurements.

Primary ions	Cs^+
Impact energy	14.5 keV
Rastered area	125 μm × 125 μm
Analysed area	60 μm in diameter
Detected ions polarity	Negative
Analyzed elements	P, Si
Mass resolution (M/DM)	3000

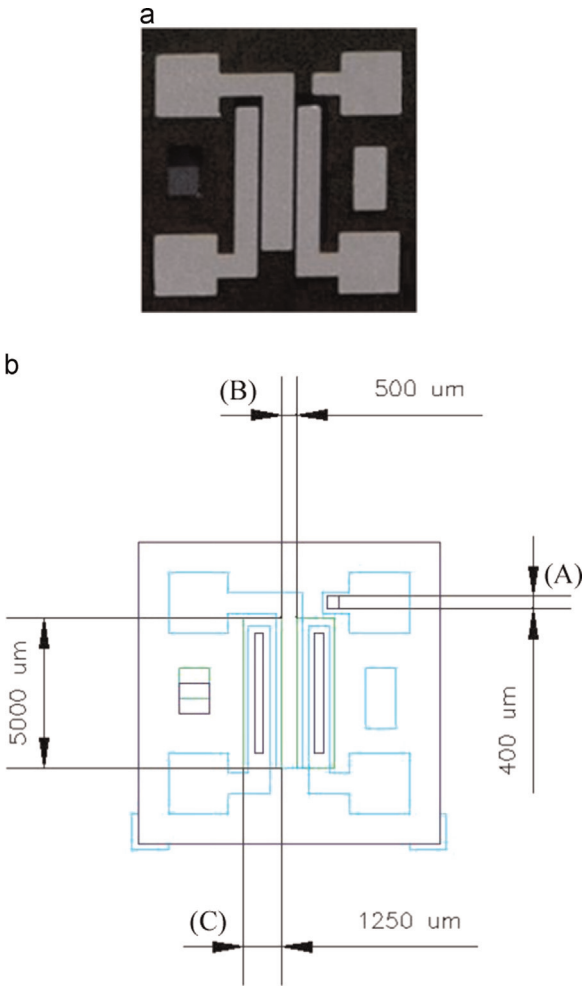

Fig. . 1. (a) Picture of the n-MOSFET (1 × 1 cm^2). (b) Masks for MOSFET fabrication, indicating: (A) back contact, (B) gate region and (C) doping zones.

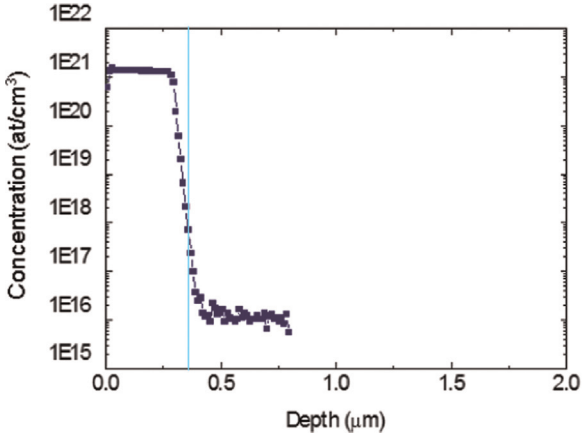

Fig. 2. Phosphorus concentration in the as-deposited a-Si:H film, 3440 Å thick (SIMS profile of sample A).

obtained from Eq. (1) [7], integrating the conductivity along the thickness to obtain the sheet conductance and inverting the expression to obtain R_S.

$$R_S = \frac{1}{q\int_0^{x_j} \mu(x)N(x)dx} \quad (1)$$