Materials Science in Semiconductor Processing 16 (2013) 1873–1878

Contents lists available at ScienceDirect

Materials Science in Semiconductor Processing

journal homepage: www.elsevier.com/locate/mssp

Alternative voltage-contrast inspection for pMOS leakage due to adjacent nMOS contact-to-poly misalignment

Hunglin Chen [a,b,*], Rongwei Fan [b], Hsiaochi Lou [a,b], Yiping Huang [a]

[a] The State Key Laboratory of ASIC & System, Department of Microelectronics, Fudan University, Shanghai 200433, China
[b] Shanghai Huali Microelectronics Corporation, Shanghai 201210, China

ARTICLE INFO

Available online 6 August 2013

Keywords:
Voltage contrast
Yield learning
e-Beam scan
Misalignment
PMOS leakage
Overlay

ABSTRACT

We propose an innovative voltage-contrast (VC) inspection approach for detection and verification of the process window for contact-to-poly overlaying. The method uses alternative scans for inline detection of leakage induced by underneath overlay drift. Conventional optical inspection with box-in-box or bar-in-bar test structures cannot accurately indicate the overall overlay performance for all chip locations as geometries continue to shrink. An e-beam inspection system with VC contrast imaging was introduced during a recent technology update. The alternative e-beam system with positive and negative charging modes was set up to perform dual scans for sensitive pMOS and nMOS detection. Although positive-mode scanning can detect pMOS leakage on the surface, it indicates a normal subsurface with no leakage. Defects can only be identified by another scan in negative mode to detect contact-to-poly misalignment in the neighboring nMOS. Leakage electrons affect each other as they spread through poly lines crossing p/nMOS. The principle and mechanisms for leakage defects were verified in a series of corrective actions for misalignment. The methodology allows inline detection instead of end-of-line electrical testing and de-layered analysis. This greatly shortens the response time and facilitates yield learning.

1. Introduction

Scanning electron microscopy (SEM) is widely used for end-of-line failure analysis of semiconductor products. By locating defect addresses in functional tests and de-layer reverse engineering for a complete device, SEM can reveal defect sources either on a high-resolution physical scale or by charge-induced voltage contrast (VC) for the material interaction. These strengths of SEM have led to widespread implementation of electron beam inspection (EBI) [1] for inline process defect inspection in semiconductor nano-technologies. The continual decrease in line width has led to lower tolerance for tiny defects, and traditional bright- or dark-field inspection cannot reveal all defects of interest (DOI). The superior resolution of EBI compensates for the limitations of conventional inspection for nanometer-scale processes.

In addition to its good physical resolution, EBI is effective in identifying device leakage. Shrinking design rules are leading to transistors that are becoming not only smaller but also closer. The small space between transistors is a challenge in process integration because different mask layers and processes must be compatible to avoid crosstalk resulting in leakage. An e-beam scan with VC image comparison is an effective method for inline leakage detection. Via SEM image observation, VC inspection can identify electron leakage via NiSi spiking in the vertical direction [2] and breakdown of intra-well isolation in the lateral direction. These leakage defects would fail end-of-

* Corresponding author at: 501 Room, No. 93, Lane 50, Guanglan Road, Pudong New Area Shanghai 201203, China. Tel.: +8613816593712; fax: +862161870100.
E-mail address: iamhlchen@gmail.com (H. Chen).

1369-8001/$ - see front matter © 2013 Elsevier Ltd. All rights reserved.
http://dx.doi.org/10.1016/j.mssp.2013.06.016

line functional tests. In traditional approaches such failures would require a series of time-consuming failure analyses to address defects linked to a single problem in a long manufacturing process. The obvious time advantage is that EBI allows inline detection instead of end-of-line electrical testing.

With the advent of 0.13-μm technology and Cu back-end processes, EBI is increasingly used for both visual and nonvisual defect inspection. Advanced semiconductor process lines tend to require many e-beam scans, especially in the early phase of technology development [3–5]. SRAM, a common process development tool [6], is suitable for electron beam scanning for in-process detection that shortens the development time. Besides product chips, EBI has been used in a dedicated sweep test for routine monitoring of line defects [7]. These typical applications detect physical defects, either very small surface defects or open/short subsurface defects. Here we extend VC inspection to detect leakage [8,9], an important electrical parameter for devices. Surface VC charging by an electron signal can identify process incoherence for contact and poly critical layers, which is only revealed by end-of-line functional tests in traditional approaches.

We present a dual-scan EBI methodology for inline detection of n/pMOS leakage. We describe the principle of positive and negative charging modes applied in wafer fabrication processes. The leakage defect mechanism is analyzed. In practice, leakage defects were verified by examination and then corrected. The approach was applied during advanced technology development, which requires wafer evaluation cycles to identify the correct path. Compared to end-of-line electrical tests, our approach provides must faster evaluation of split experiments and hence shortens the development period when ramping up yields.

2. VC inspection

2.1. Positive and negative charging

VC inspection is typically used to detect subsurface open/short defects, but here we extend its application to electrical leakage. Open/short defects accumulate or dispense a certain number of electrons and project a clear VC image. In contrast, electrical leakage, involving undesirable dispensing of a small number of electrons, usually shows little signal variance and a weak VC image. The image can be enhanced by dedicated setting of the electron beam column.

Wafer surface charging is triggered by electron beam treatment in positive or negative mode, depending on the landing energy (E_L) of the electron landing material. When electrons in the focused primary beam hit a tiny spot on the wafer surface, many secondary and backscattered electrons, as well as some other electrons and photons, are excited. Fig. 1 shows the relationship between yield and E_L for secondary and backscattered electrons. The relationship can be expressed as

$$\sigma(E_L) = 1 - \frac{E_L - E}{I_p R}, \quad (1)$$

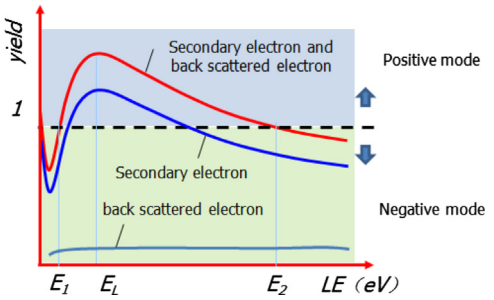

Fig. 1. Yield rate versus landing energy (LE) for the primary beam for secondary electrons, backscattered electrons, and their combination.

where σ is the electron yield rate, E_L is the landing energy, I_p is the probe current, and R is the material resistance. For an ideal insulator, $\sigma(E_L)$ and $E_L = E_2$; for a metal, $R \to 0$ and $\sigma \to 0$, and the surface has no charge.

The dashed line in Fig. 1 indicates a yield of 1 and the crossover points at E_1 and E_2 denote the boundary for surface charging inversion. E_1 is very low for most materials and the corresponding electron image is poor. Therefore, electron beam systems are not usually operated at E_L values less than E_1. For E_L between E_1 and IE_2, the yield is >1, which means that more electrons leave the surface than reach it. Thus, the surface is positively charged. By contrast, the yield for a negatively charged surface is <1. Fewer electrons leave the surface than reach it, and the corresponding E_L is greater than E_2. Positive and negative charging modes are proposed for detecting leakage in CMOS transistors and VC images for nMOS and pMOS transistors are explained in the next section.

2.2. Scan steps

A front-of-line process is used to fabricate CMOS device features; however, most scan steps for VC inspection are at the middle of the line, after W CMPs in the contact layer. In the process, after W CMPs, each W conducting plug is separated by an oxide insulating film surrounding and landed on different regions of the device, such as source/drain and poly gates for n/pPMOS contacts. This is suitable for distinguishing VC images. The scan area contains conventional six-transistor SRAM cells. The three different landing structures for W plus connections are p+/n-wells in pMOS contacts, n+/p-wells in nMOS contacts, and poly gates. Because each structure has unique electrical characteristics, the VC images exhibit different grayscale levels. The feature is ideal for VC inspection.

Fig. 2 shows the VC appearance on top of W plug connections on the pMOS shared contact, the pMOS alone, the nMOS alone, and the floating poly gate. Under normal conditions without leakage, both positive and negative charging modes exhibit a similar appearance: pMOS contacts are bright while nMOS contacts are dark (Figs. 2a, and b). However, when nMOS leakage occurs, a VC change is observed in positive mode but is invisible in negative mode (Fig. 2c) and *vice versa* when pMOS leakage occurs (Fig. 2d). A dual scan with positive and negative modes is