



Industrial high-speed wireless synchronous data acquisition system with real-time data compression



Yazhou Yuan ^{a,b}, Qimin Xu ^{a,b}, Xinping Guan ^{a,b}, Zhixin Liu ^{b,*}

^a School of Electronic, Information and Electrical Engineering, Shanghai Jiaotong University, Shanghai 200240, China

^b Center for Networking Control and Bioinformatics, Institute of Electrical Engineering, Yanshan University, Qinhuangdao 066004, China

ARTICLE INFO

Article history:

Received 17 September 2012

Accepted 25 June 2013

Available online 3 July 2013

Keywords:

Wireless data acquisition system

Synchronous acquisition

Data compression

ABSTRACT

In this paper, an industrial wireless data acquisition system (WDAS) is presented. This system aims to change the inflexibility of wired system and improve the wireless transmission rate. First, the WDAS system consists of one wireless gateway and some wireless data acquisition terminals (WDAT), and IEEE 802.11n protocol is used to construct a multipoint distribution network. Then, in order to simplify the synchronous method and the data packet structure, we design a synchronous solution which adopts the console aided control method. The adaptive frequency and amplitude (AFA) compression algorithm is employed to reduce the data redundancy. Consequently, system can transmit more data by limited bandwidth. Last, some experiments of the compression algorithm are given to show the effectiveness of the AFA algorithm. By using the proposed system, distributed signals are synchronously measured and, hence, real-time analysis can be realized.

© 2013 Elsevier Ltd. All rights reserved.

1. Introduction

Data acquisition system (DAS) has been widely used in many fields such as engine diagnosis, safeguard applications, power quality analysis and so on [1]. Most of the DASs use wired network to transmit data. They are high cost and not flexible enough [2]. Using wireless solutions reduces data acquisition cost and permits easy expansion for measurement points. It allows connection to the point that is physically or economically difficult to access. Thus, wireless data acquisition system (WDAS) is desirable. Many studies have investigated Wireless Data Acquisition technologies. Some solutions [3–5] are based on Zigbee protocol, GPRS and so on. The data bandwidths of them range from 20 kb/s and 250 kb/s. Hence, they do not suit for those applications which require large bandwidth. To meet the bandwidth requirement, the wireless scheme is introduced in this paper, which utilizes IEEE 802.11n protocol to implement high-speed transmission.

In order to analyze information precisely at a distribution system in some fields such as power quality analysis, safeguard application [6,7], the WDAS is required to be able to synchronously measure the signals at each point. Because the error of IEEE 1588 is bigger than the Global Positioning System (GPS) [8], GPS is used to be the main synchronizing source which provides a accurate sampling clock on the WDATs. In this paper, to simplify the synchronous method and the data packet structure, we present an optimal synchronous solution to realize precise synchronization. In this solution a compact coding format for time information is used instead of the universal coordinate time (UTC) time information. Moreover, the console aided control method is adopted to realize the synchronization of all the WDATs.

The sampled data before processed is in large quantities. For example, if the system has 5 WDATs, a data acquisition of 30 min with a 50 kHz sampling rate and 16 bits resolution requires about 0.88 Gbytes of storage. In addition, the available bandwidth of the WDAT is limited. Therefore, the data compression algorithm is necessary. the compression rate of algorithm is a very important parameter [9] because of the large data transmit and

* Corresponding author. Tel.: +86 15032385957.

E-mail address: lzxauto@ysu.edu.cn (Z. Liu).

compression in the embedded platform. Considering these factors, we employ the adaptive frequency and amplitude (AFA) algorithm due to the non-optimized sampling frequency [1] and sampled data bits [10]. And some experiments of the algorithm are run in the WDAT.

The paper is organized as follows: in Section 2, the brief system structure of the proposed WDAS is introduced; Section 3 presents the details of the WDAS; in Section 4, the performance of the AFA algorithm is analyzed. Finally, the conclusions are drawn in Section 5.

2. Brief structure of wireless data acquisition system

The block diagram of the overall system is illustrated in Fig. 1. The WDAT is assigned to the measure points to acquire and process the signals in real time. It consists of an AM3517 processor (ARM Cortex A-8 core) for data process, a CPLD for sampling control, a GPS for time synchronization, and a wireless network card for data transmission. AM3517 processor is a high-performance industrial application microprocessor and it runs at up to 600 MHz. The data after process is transferred to the console. And the console is comprised of the wireless gateway and the high-end computer. The high-end computer communicates with the wireless gateway by Ethernet. The WDAT prototype is shown in Fig. 2.

3. System description

3.1. Data acquisition and wireless transmission

N analog signals are connected to n fast ADCs which are all controlled by CPLD. To have fast sample rate, the system uses 16 bit AD7663 as the ADC. The ADC sampling clock is

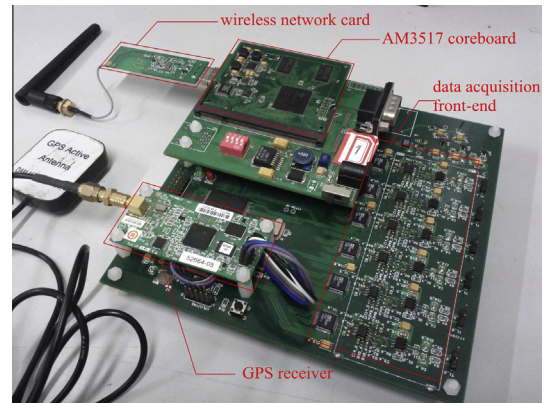


Fig. 2. WDAT prototype.

outputted from dividing-frequency circuit based on the CPLD as well. And the clock signal source is a Pulse-Per-Second (PPS) timing signal of the GPS receiver synchronizing to the UTC with high accuracy. Trimble's Resolution T GPS Timing Receiver used in our system has accurate 1-PPS output, synchronized to UTC within 15 ns (one sigma). By using the PPS signal as the external sampling clock source of the ADC, the WDATs share a common time source with an established accuracy.

During acquisition, the continuous data stream coming from the ADCs is temporarily stored in the FIFO, which is a memory pool for buffering. When the FIFO is full, the sampled data are transferred to the SDRAM by the direct memory access (DMA) interrupt without microprocessor unit (MPU) support.

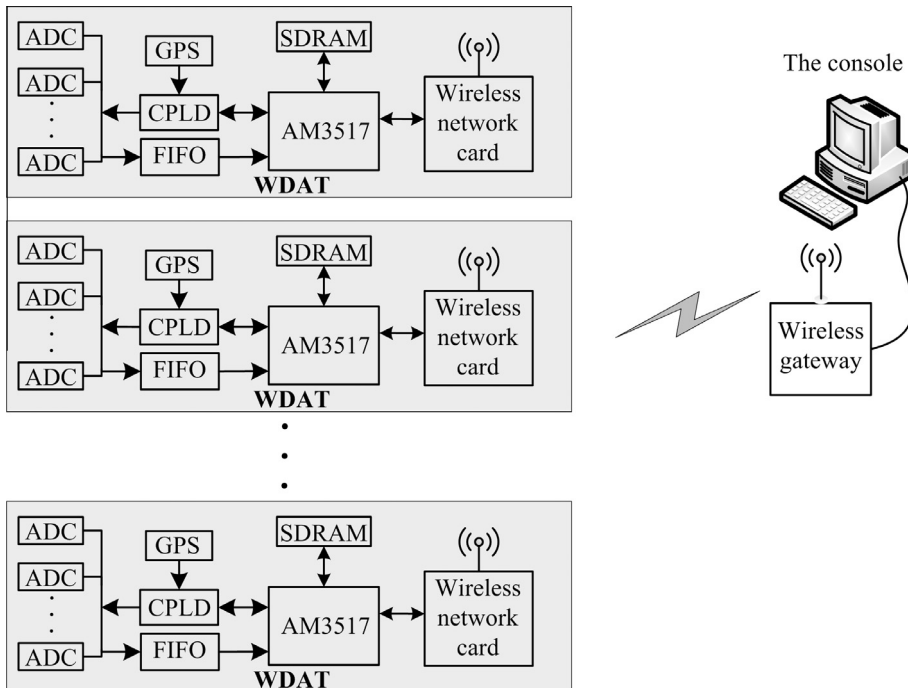


Fig. 1. System architecture.

Download English Version:

<https://daneshyari.com/en/article/10407352>

Download Persian Version:

<https://daneshyari.com/article/10407352>

[Daneshyari.com](https://daneshyari.com)