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Wafer-level bonding and direct electrical interconnection of stacked 3D MEMS by a hybrid low temperature process

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ABSTRACT

The presented fabrication technology enables the direct integration of electrical interconnects during low temperature wafer bonding of stacked 3D MEMS and wafer-level packaging. The low temperature fabrication process is based on hydrophilic direct bonding of plasma activated Si/SiO_2 surfaces and the simultaneous interconnection of two metallization layers by eutectic bonding of ultra-thin AuSn connects. This hybrid wafer-level bonding and interconnection technology allows for the integration of metal interconnects and multiple materials in stacked MEMS devices. The process flow is successfully validated by fabricating test structures made out of a two wafer stack and featuring multiple ohmic electrical interconnects.

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1. Introduction

There is a growing interest in improving the performance and functionality of MEMS by integrating different materials combined with high-aspect-ratio 3D silicon structures fabricated by wafer stacking [1–3]. The integration and electrical connection of metal electrodes for actuation and sensing on multiple device layers is challenging and an important factor for cost and reliability issues [4,5]. In addition, 3D MEMS with integrated polymer layers or mechanical structures set even more challenging process temperature requirements, typically below 300 °C, than CMOS/MEMS integration. Therefore, established wafer stacking technologies, based on anodic or fusion bonding cannot be applied due to the related elevated process temperatures. The use of microheaters for local fusion and eutectic bonding is an approach to keep the overall substrate temperature low [6]. Though, the microheater integration on MEMS substrates adds substantial process complexity and is not applicable to stacked 3D structures in a straight forward way. One prominent approach allowing for bonding and interconnection relies on combined adhesive and metal bonding [7,8]. However, the planarization of heterogeneous substrates is challenging and may not be compatible with already structured MEMS device substrates, e.g. cavities or suspended structures.

Further, there is multitude of different approaches for layer transfer and interconnection developed for 3D-integrated circuit (3D-IC) fabrication [9,10]. Most of these technologies are therefore not optimized for an application in 3D MEMS stacking. For example, a layer transfer and interconnection method based on polyimide temporary bonding and CuSn via technology [11], has the drawback of thick interconnects deposited by electroplating, an annealing temperature of 380 °C as well as a thick adhesive bonding layer. Recent advances in 3D-IC technology demonstrated the potential of metal direct bonding for the stacking and interconnection of ICs [12]. Like the combined adhesive and metal bonding, this technology involves a demanding planarization process for adequate mechanical and electrical properties. On the other hand, Cu–Cu thermo-compression bonding requires an annealing at elevated temperatures in order to allow Cu inter-diffusion and grain growth to achieve high enough bonding strength and low number of interfacial voids [13]. A commercial technology for CMOS/MEMS integration and cavity sealing is based on eutectic Al–Ge bonding but requires similar elevated annealing temperatures, since the Al–Ge eutectic point is around 420 °C [14]. Other approaches are based on solder bonding, which enables void free bonding at low temperatures [5,15,16]. However, the relatively thick solder metallization of several microns has to be deposited by electroplating and additional process steps are required for a precise bond gap control [5].

In this paper we present a hybrid fabrication technology allowing for wafer-level bonding and direct electrical interconnection of metallization layers in one low temperature process not exceeding 300 °C. The process does not require any planarization to locally connect different materials and layers of substrates featuring MEMS structures. The hybrid bonding process combines hydrophilic direct bonding and the simultaneous eutectic bonding of AuSn interconnects. The direct bond covers the same functionality as distance holders used in [5], but additionally creates a

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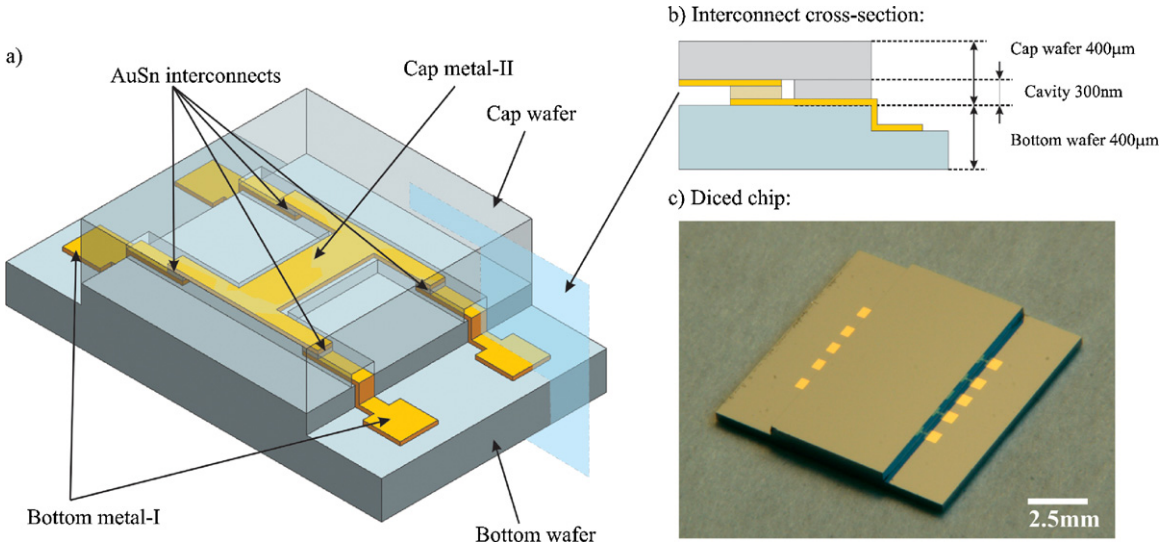

Fig. 1. (a) Schematic CAD drawing of the test structure showing the two complementary metallization layers and the AuSn interconnects (the cap wafer is transparent for a better visibility of the structure), (b) cross-section of the two wafer stack with vertical dimensions, (c) photograph of a fabricated test structure showing the probing pads and the bonded cap.

mechanical bond between the substrates. This strong mechanical bond is performed by hydrophilic direct bonding of plasma activated Si and SiO_2 interfaces [17,18]. The prevailing bonding mechanism is the polymerization of hydroxyl functional groups which form strong covalent siloxane bonds [19]. Simultaneously ultra-thin AuSn contact pads are forming local electrical interconnects between the metallization layers of the two bonded substrates. Since the electrical interconnect is formed by local eutectic bonding and reflow of the AuSn metallization, no substrate planarization by CMP is required before bonding. Further, the combination of direct bonding and the local eutectic AuSn bonding for interconnection has the inherent advantage of precise vertical gap control and is taking advantage of the mechanical and electrical properties of each specific material or boning technology, respectively. Due to the overall process temperature not exceeding 300 °C, the technology also allows for the integration of polymer structures in stacked 3D MEMS.

The fabrication process flow for bonding and interconnecting multiple layers in stacked 3D MEMS and packaging, is demonstrated by fabricating test structures. The structures are made out of a two wafer stack were each layer is featuring a metallization deposited into an etched cavity. These two complementary metal layers are then locally connected by the vertical AuSn interconnects. The CAD drawing in Fig. 1 shows the generic test device design (a), an interconnect cross-section of the indicated plane (b), as well as a picture of a fabricated chip (c). The validation concept is

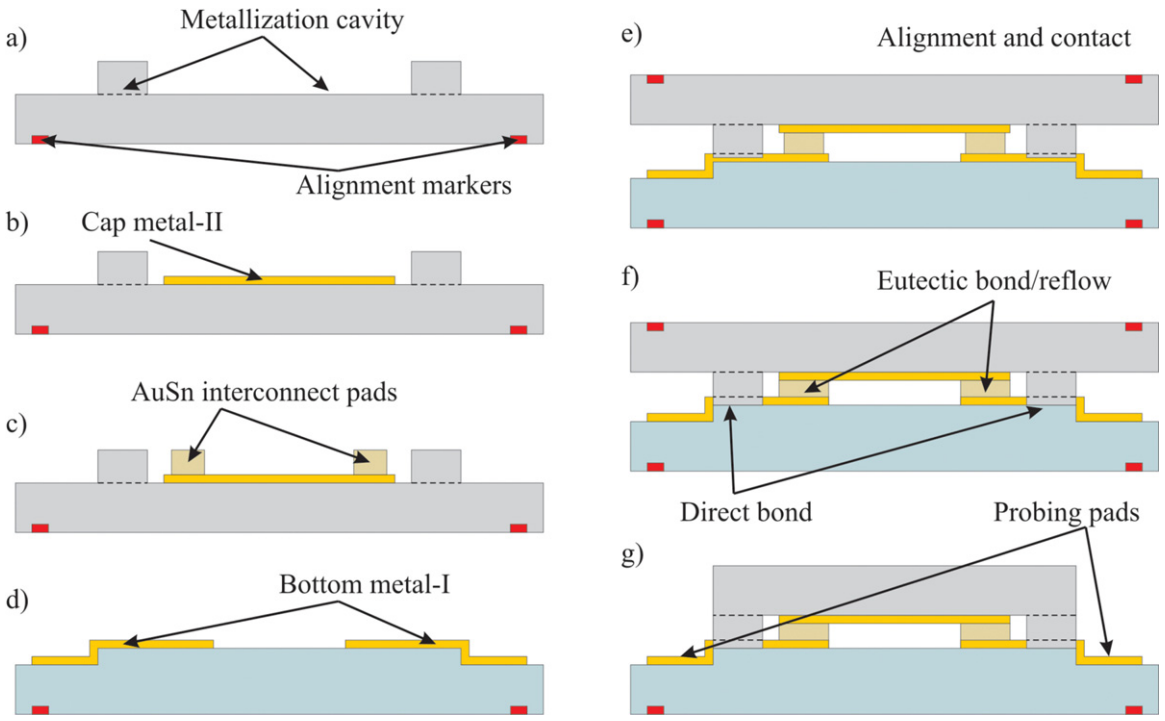

Fig. 2. Fabrication process flow showing the preparation of the cap wafer (a–c), the bottom wafer (d) as well as the low temperature hybrid bonding process (f).

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