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Micromachined DC contact capacitive switch on low-resistivity silicon substrate

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Abstract

A DC contact capacitive shunt switch on low-resistivity Si substrate is designed and demonstrated. There are two main differences between this design and the conventional capacitive shunt switch. First, the dielectric layer is fabricated on the ground planes of the coplanar waveguide (CPW) transmission line. The contact between the metal bridge and the center conductor becomes DC contact when the metal bridge is driven down. As a result, the down-state capacitance degradation problem can be solved and the down-state capacitance as high as 30 pF can be achieved. Second, the switch is fabricated on a low-resistivity silicon substrate. This is the first time where a RF MEMS switch can be fabricated on a low-resistivity silicon substrate without any wafer transfer technology; thus, it can greatly simplify the fabrication process and reduce cost. Measurement results show that the insertion loss is lower than 0.4 dB until 26.5 GHz and the isolation is 15 dB at 1 GHz, 26 dB at 10 GHz and 27 dB at 26.5 GHz. The down-state resistance and the inductance are 1.3 Ω and 2 pH, respectively.

Keywords: DC contact switch; Capacitive shunt switch; CPW transmission line; RF MEMS

1. Introduction

An important figure of merit qualifying the RF performance of a capacitive switch is the down/up capacitance ratio *R*. However, for most of the capacitive shunt switch reported to date, it is difficult to obtain capacitance ratio larger than 150 because of the down-state capacitance degradation problem, which means that the obtained down-state capacitance is much smaller than the designed value. As a result, conventional capacitive shunt switches are more suitable when frequency is higher than X-band (8–12 GHz) because it is difficult to obtain larger than 15 dB isolation at lower frequency range [1].

To obtain high isolation in or lower than X-band, one method is to use inductively tuned capacitive switches by properly choosing the *LC* resonant frequency; however, the bandwidth of this design is narrow because of the large down-state inductance in the circuit [2]. Another method is to use dielectric material with high dielectric constant, such as strontium titanate oxide (STO) with a relative dielectric constant ranging between 30 and 120 [3]. Large capacitance ratio of 600 is obtained, and higher than 30 dB isolation can be achieved at 2 GHz. However, the STO material is not a commonly used material in MEMS fabrication process, and the down-state capacitance is greatly degraded as the designed capacitance ratio is larger than 1000. The down-state capacitance degradation problem is caused by the non-planar metal bridge, roughness of the contact area and the etching hole in the metal bridge etc. [4]. To avoid this problem, a switched-capacitor approach can be used [5,6], in which a metal–insulator–metal (MIM) capacitor is defined between the bridge and the coplanar waveguide (CPW) center conductor. This results in a capacitance ratio that is independent of the roughness of the bottom electrode. However, in this design, the MIM capacitor is defined on the CPW center conductor, therefore, its capacitance value is limited by the width of the CPW center conductor.

Another problem in most recently reported capacitance shunt switches is that in order to reduce substrate loss, these switches need to be fabricated on low loss substrates, as done on high-resistivity silicon substrates, glass or quartz substrates, or to use wafer transfer technique [7]. Either method has its respective

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shortcoming(s). For instance, the silicon, glass or quartz substrates are more expensive compared to the low resistivity silicon substrate, whereas use of the wafer transfer technique will complicate the fabrication process.

The objective of this paper is to develop a DC contact capacitive shunt switch without down-state capacitance degradation problem, and to use low resistivity silicon as substrate without any wafer transfer process. First, the design of the capacitive switch with the dielectric layer patterned on the ground planes of the CPW is presented. It is shown that by shifting the dielectric layer onto the ground planes of the CPW transmission line, the down-state capacitance degradation problem can be avoided and high capacitance ratio can be obtained. It is also shown that by properly selecting the dimensions of the CPW transmission line, it is feasible for this switch to be fabricated on a low-resistivity silicon wafer. Second, the fabrication process of this switch is proposed, a SiO_2 layer with thickness of 18 μm is deposited on the silicon substrate as isolation layer. Finally, the measurement results are presented and discussed.

2. Switch design and modeling

2.1. Design of DOG switch

Fig. 1 shows a schematic diagram of the newly designed switch. In this design, the dielectric layer is fabricated on the CPW ground planes instead of the CPW center conductor. The metal bridge, the dielectric layers and the CPW ground planes consist of two MIM capacitors in shunt connection. Because of the nature of its construction, this newly designed switch is referred as dielectric-on-ground (DOG) switch while the conventional capacitive switch is referred as dielectric-on-center conductor (DOC) switch in this paper.

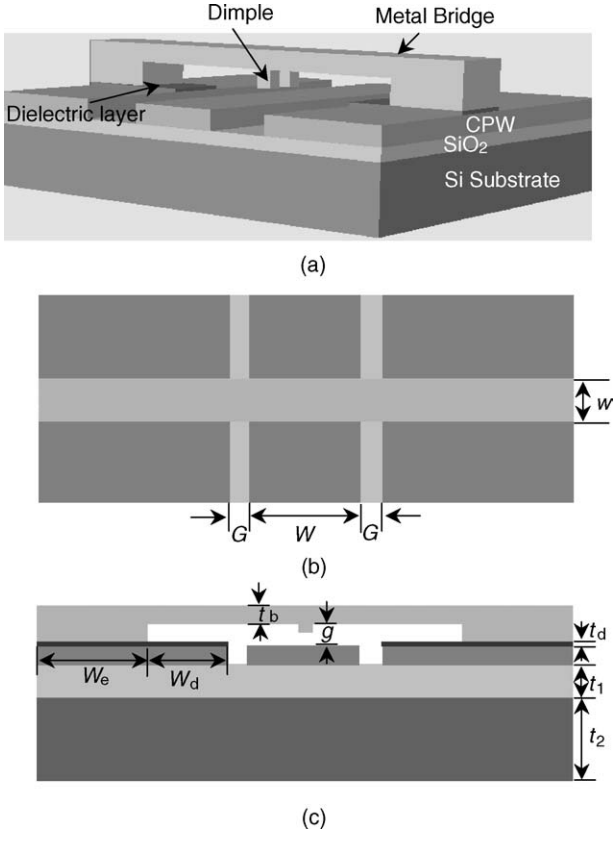

Fig. 1. Schematic diagram of the DOG capacitive switch: (a) 3D view; (b) top view; (c) cross section view.

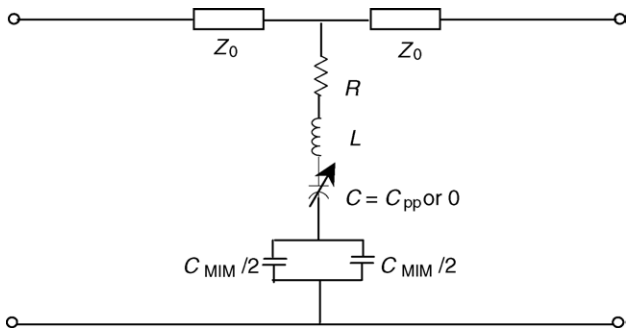

Fig. 2. Equivalent circuit of DOG switch.

Fig. 2 shows the equivalent circuit of the switch. In the up-state position, the switch capacitance C_u^{DOG} is dominated by the parallel-plate capacitance C_{pp} between the metal bridge and the CPW center conductor, that is:

$$C_u^{DOG} \cong C_{pp} = \frac{\varepsilon_0 A_1}{g + t_d/\varepsilon_r} \cong \frac{\varepsilon_0 A_1}{g} \tag{1}$$

where A_1 is the overlap area between the metal bridge and the CPW center conductor and $A_1 = wW$ with w is the width of the metal bridge and W is the width of the CPW center conductor.

While in the down-state, the DC-contact between the metal bridge and the CPW center conductor results in an R_sL model in series with MIM capacitors. Therefore, the down-state capacitance of the switch C_d^{DOG} is dominated by the capacitance of the MIM capacitor C_{MIM}, that is:

$$C_d^{DOG} = C_{MIM} = \frac{\varepsilon_0 \varepsilon_r A_2}{t_d} \tag{2}$$

where A_2 is the total area of the MIM capacitor and $A_2 = 2wW_d$ with W_d is the width of the MIM capacitor.

Therefore, the capacitance ratio of this DOG switch can be expressed as:

$$r = \frac{C_d^{DOG}}{C_u^{DOG}} = \frac{\varepsilon_r g}{t_d}\frac{A_2}{A_1} = r_0 \frac{A_2}{A_1} \tag{3}$$

where $r_0 = \frac{\varepsilon_r g}{t_d}$ is the capacitance ratio for the DOC switch.

From Eq. (3), for the DOG switch, high capacitance ratio can be obtained by increasing A_2/A_1, which gives a new degree of freedom to optimize the switch design, and no down-state capacitance degradation problem would occur. This is one of the advantages from this DOG switch.

It is interesting to note that since the MIM capacitor is defined on the ground planes of the CPW transmission line, the width of the CPW slots can be reduced to 20 μm or narrower while the characteristic impedance Z_0 of the CPW transmission line can still be maintained as 50 Ω by properly selecting the width of the