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Design and optimization of junction termination extension (JTE) for 4H–SiC high voltage Schottky diodes

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Abstract

This paper analyzes single- and double-zone junction termination extension (JTE) structures for 4H–SiC Schottky diodes using numerical simulations. In the single-zone case, we study the effects of JTE dose, depth, length, metal/JTE overlap length, and surface or interface charge. In the double-zone case, we systematically vary the inner and outer doses over about 80 possible combinations for each of three sets of inner and outer zone widths. The total JTE width is constrained to be that necessary for optimum breakdown voltage in the single-zone case. The results are presented as contour plots of breakdown voltage and maximum surface field as a function of the two doses, with the locations of peak bulk and surface fields also indicated at each point. The resulting tolerance to variations in activated dose can then be visualized directly. The physics underlying the shapes of the contours is explained in some detail. We show that JTE behavior is significantly different for Schottky diodes compared to the better-known case of *p*(*i*)*n* junction diodes. The peak surface field is *increased* for Schottky diodes when the single-zone dose is reduced below its optimum value, which is opposite to the behavior of *pn* junctions. Moreover, double-zone JTE is not effective in reducing peak surface field for the Schottky case, unlike *pn* junctions, although tolerance to dose variations can be improved with two zones. The usual rule of thumb for double-zone JTE design for *pn* junctions is not appropriate for Schottky diodes, because of the field crowding near the sharp metal edge. We recommend an inner dose of 95–105% of the ideal single-zone and an outer dose of 70–80% of the single-zone value, with a width ratio of ∼1:1 for the inner and outer zones and a total width similar to the optimal value in a single-zone design.
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1. Introduction

Silicon carbide is currently of great interest for high voltage power devices. Its properties of high critical field strength, reasonable carrier mobilities, wide bandgap, and high thermal conductivity make it a useful material for high frequency, high temperature, and high power devices. Due to its higher mobility along the *c*-axis compared to the 6H polytype, the 4H–SiC polytype is better suited for vertical power devices [1]. The design of power devices with thinner and more highly doped epilayers is possible due to high critical breakdown field, drastically reducing on-resistance [2]. Power devices are required to have excellent voltage blocking capabilities, high current ratings, high reliability, and good thermal characteristics. In high voltage devices, avoiding premature breakdown is a key issue. Due to three-dimensional junction curvature effects and electric field crowding near the

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Nomenclature

N_D epilayer doping in cm^{-3}
N_S substrate doping in cm^{-3}
N_A JTE region doping in cm^{-3} for a single-zone JTE
N_{A1} JTE_1 region doping in cm^{-3} for a double-zone JTE
N_{A2} JTE_2 region doping in cm^{-3} for a double-zone JTE
d depth of JTE region(s)
W width of single-zone JTE region
δ Schottky metal overlap
W_1 width of JTE_1 region
W_2 width of JTE_2 region
V_{br} breakdown voltage

edge of the junction, unterminated planar devices exhibit very low breakdown voltages as compared to ideal one-dimensional device structures. Therefore, junction termination methods are very important to attain high breakdown voltages.

Various edge terminations such as metal field plates [3,4], floating field-limiting rings [5], buried field rings [6], guard rings [7], a high resistivity layer termination [8], junction termination extension (JTE) [9,10], mesa-JTE [10], graded JTE [11], multi-step JTE (MJTE) [12], field plate-junction termination extension (FP-JTE) [13], SIPOS layers [14], oxide ramp termination [15], and edge beveling [16] have been explored for SiC power devices. The choice of a particular termination technique depends on the desired blocking voltage range, the available semiconductor surface area, and trade-offs involving the complexity of the technological process [17]. The JTE termination technique proposed by Temple and Tantraporn [18,19] is one of the most widely used and effective techniques for SiC devices. Field plates are not reliable for devices with more than 2 kV blocking voltage devices because at high voltages, the barrier to electron tunneling is reduced at the SiC-SiO_2 interface due to the high fields present in the oxide layer [16]. Guard rings require deep diffusion of dopants to create sufficiently large cylindrical junctions to minimize field crowding, and are not very suitable for SiC devices due to the very low diffusivity of dopants in this material. The JTE and multiple-zone JTE (MJTE) structures are considered favorable for SiC devices due to nearly ideal breakdown voltages, ease of fabrication, and the resulting reduction in surface fields in the case of *pn* junctions [16]. An additional advantage of the JTE structure is that it can be scaled to higher voltages without increasing the implanted JTE layer junction depth [16].

Schottky barrier diodes (SBDs) made on 4H–SiC are attractive because they provide rectification without significant switching losses and with no reverse recovery transients, unlike *pn* junctions. Moreover, the forward voltage drop of a SiC *pn* junction diode is proportional to the bandgap and is therefore relatively large. Schottky diodes made on SiC are particularly useful because Schottky contacts with sufficiently large barrier heights can be made. Also, these devices have forward voltage drops proportional to the Schottky barrier height, which can be significantly less than the bandgap [20]. The low forward voltage drop of a Schottky diode and the lower reverse leakage current of a *pn* junction can be achieved simultaneously in more complicated structures, such as junction barrier Schottky (JBS) and merged *pn* Schottky (MPS) rectifiers [20,21]. In the present study, we focus exclusively on planar SBDs using implanted terminations. More complicated structures may be considered in future work.

In the past few years, several authors have reported design and fabrication of very high voltage 4H–SiC rectifiers [22–25]. Schottky diodes on 4H–SiC with 4 kV blocking voltages were reported by McGlothlin et al. [22]. Sugawara et al. demonstrated 4H–SiC ultra high voltage *p-i-n* diodes with breakdown voltages up to 12–19 kV [23]. The first 10 kV 4H–SiC Schottky barrier diodes were reported by Zhao et al. [24]. Wang and Cooper simulated a triple-zone JTE for a 10 kV *p-i-n* power diode in 4H–SiC [25]. Most of these authors used JTE terminations in their designs but none of them has discussed the optimization of the JTE in detail, and systematic studies of modeling and simulation of JTE for 4H–SiC Schottky diodes are rare. Extensive simulations of JTE have been performed for 4H–SiC *p-i-n* junctions [9,10,22,26,27], but similar simulations for JTE of 4H–SiC Schottky diodes have been much less extensive [28]. Moreover, most studies of the JTE method in other materials have also focused exclusively on *p-i-n* junctions [18,19], and not on Schottky diodes. As we show in the following, the design considerations for Schottky diodes and *p-i-n* diodes are substantially different.

In this paper, we study the design of single- and double-zone JTE for 4H–SiC Schottky diodes. The general principles and results we deduce are however applicable to JTE of Schottky diodes on any semiconductor material. Optimization of JTE parameters and knowledge of the sensitivity of breakdown voltage to variations in each parameter is critical to obtain a suitable edge termination for any type of JTE-terminated device. We performed extensive analysis of the effects of JTE

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