Available online at www.sciencedirect.com
SCIENCE DIRECT®
Solid-State Electronics 49 (2005) 986–990
SOLID-STATE ELECTRONICS
www.elsevier.com/locate/sse

The effects of mechanical planar biaxial strain in Si/SiGe HBT BiCMOS technology

Becca M. Haugerud [a,*,1], Mustayeen B. Nayeem [a], Ramkumar Krithivasan [a], Yuan Lu [a], Chendong Zhu [a], John D. Cressler [a], Rona E. Belford [b], Alvin J. Joseph [c]

[a] Department of Electrical and Computer Engineering, Georgia Institute of Technology, 777 Atlantic Drive N.W., Atlanta, GA 30332-0250, USA
[b] Belford Research Inc., Hilton Head, SC 29926, USA
[c] IBM, Essex Junction, VT 15452, USA

Received 30 October 2004; received in revised form 22 February 2005; accepted 19 March 2005

The review of this paper was arranged by Prof. A. Zaslavsky

Abstract

This work presents the results of the effects of mechanical planar biaxial tensile strain applied, post-fabrication, to Si/SiGe HBT BiCMOS technology. Planar biaxial tensile strain was applied to the samples, which included both standard Si CMOS, SiGe HBTs, and an epitaxial-base Si BJT control, for both first and second generation SiGe technologies. Device characterization was performed before and after strain, under identical conditions. At a strain level of 0.123%, increases in the saturated drain current as well as effective mobility are observed for the nFETs. The Si BJT/SiGe HBTs showed a consistent decrease in collector current and hence current gain after strain.

Keywords: Mechanical; Biaxial; Strain; Si BJT; SiGe HBT; CMOS

1. Motivation

Straining silicon is widely recognized as a potential alternative to dimensional scaling for enhanced CMOS performance. Several publications have demonstrated significant drain current improvements (10–30%) associated with increased carrier mobility. Strain induced from Si–SiGe lattice mismatch, as well as process-induced strain, has been explored by various groups [1]. In the Si–SiGe lattice mismatch method, the Si channel is under biaxial strain. Some limitations of this method are Ge migration, high defect density and larger percentage of strain requirement for any pFET enhancements. Process-induced strain, either uniaxial or biaxial, can be used to optimize nFET and pFET devices on the same wafer independently by applying different levels of strain [2].

A third way of inducing strain is mechanical, which is presented here. This method is applied post-fabrication, unlike the two other techniques mentioned above [3,4]. Both uniaxial and biaxial strain can be realized in this manner. Previous work has studied the effects of uniaxial mechanical strain on MOSFET devices [3]. Although much work has been done on the MOSFET devices, very few attempts have been made to investigate the effects of strain on the modern Si BJT and SiGe HBTs [5]. In this work, we report results of mechanical planar biaxial tensile strain applied to a Si/SiGe HBT BiCMOS technology. Unlike the other mechanically induced

* Corresponding author. Tel.: +1 404 894 5161; fax: +1 404 894 4641.
E-mail address: becca@ece.gatech.edu (B.M. Haugerud).
[1] This work was supported by DARPA, IBM, and The Georgia Electronic Design Center at Georgia Tech.

0038-1101/$ - see front matter © 2005 Elsevier Ltd. All rights reserved.
doi:10.1016/j.sse.2005.03.019

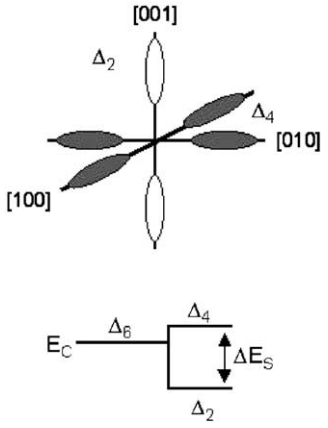

Fig. 1. Conduction band splitting for biaxial strain.

strain experiments, Si BJT/SiGe HBT and Si CMOS devices are biaxially strained together on the same die. Biaxial strain is known to alter both the conduction and valence bands of Si. Fig. 1 illustrates the biaxial strain induced splitting of the previously degenerate Si conduction band. In the valence band, biaxial strain reduces the heavy hole and split off band energies with respect to the light hole band. The strain alters the shape of valence bands, while leaving the shape of the conduction bands unchanged [6].

2. Device technology and experiment

Three fully integrated BiCMOS technologies were investigated in this study: a 0.50 μm, 50 GHz peak f_T SiGe HBT BiCMOS, the 0.35 μm standard Si CMOS on this technology platform (strained together on the same die for unambiguous comparisons), a 0.50 μm epitaxial-base Si BJT control (fabricated identically in the same wafer lot as the SiGe HBT), the 0.35 μm standard Si CMOS on this technology platform (identical to the Si CMOS on the SiGe HBT wafer), and a 0.18 μm 120 GHz peak f_T SiGe HBT BiCMOS, with three distinct 0.18 μm Si CMOS device versions [7,8]. A schematic cross-section of the Si/SiGe BJT/HBT and CMOS devices (nFET) is depicted in Fig. 2. These wafers were diced and thinned to (flexible) membrane dimensions (⩽25 μm thickness). Planar biaxial strain was achieved by using a novel differential thermal bonding technique [9,10], in which the thinned membrane is bonded to a substrate of different coefficient of thermal expansion (CTE) at high temperature.

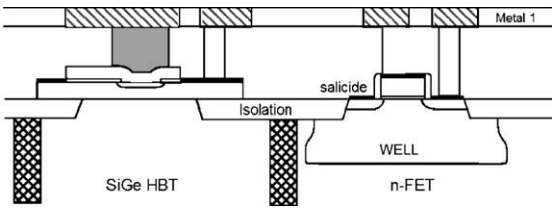

Fig. 2. Schematic cross-section of the SiGe HBT BiCMOS technology.

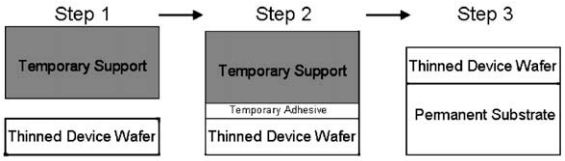

Fig. 3. Process flow for the planar biaxial strain by differential thermal bonding.

The biaxial strain is induced as the bonded pair returns to ambient temperature (see Fig. 3). The applied biaxial tensile strain was calculated to be 0.123%. Pre- and post-strain measurements were carefully made using an Agilent 4155 Parameter Analyzer.

3. CMOS results

Fig. 4 depicts the output characteristics of a 1.8 V, high V_T, 10×10 μm nFET as well as a 3.3 V, 10×0.5 μm pFET. In the case of the nFET, there is a 9.52% increase in the saturation current (I_{sat}), as well as a reduction in channel resistance after strain. We see that the applied strain has decreased the pFET saturation current by approximately 2.93%. Fig. 5 illustrates the corresponding nFET and pFET transfer characteristics for pre- and post-strain, on a linear scale. The effective mobility ($\mu_{eff} = g_d/((W/L)Q_i)$) versus effective field (E_{eff}) for a 1.8 V, high V_T, 10×10 μm nFET and a 3.3 V, 10×0.5 μm pFET are shown in Fig. 6. After strain, the nFET μ_{eff} is improved by 9.54%, however there is a degradation in the pFET μ_{eff} after strain.

The enhanced nFET performance with strain is attributed to the reduction of both the in-plane effective mass and intervalley scattering [11,12]. Our results indicate that pFET performance, in general, tends to degrade with this method of induced tensile biaxial

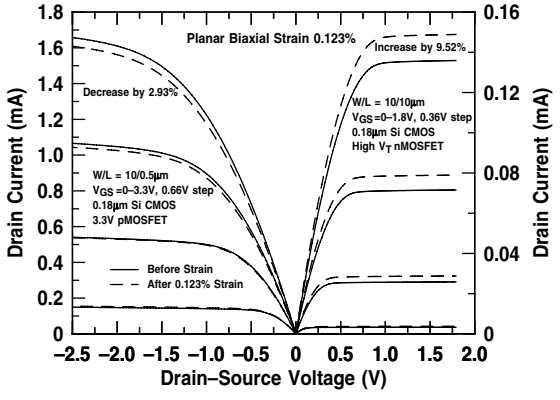

Fig. 4. nFET and pFET output characteristics for both pre-strain and post 0.123% strain.