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Electron mobility in ultra-thin InGaAs channels: Impact of surface orientation and different gate oxide materials

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ABSTRACT

Electron mobility is investigated in sub-20 nm-thick InGaAs channels, sandwiched between different gate oxides (SiO_2, Al_2O_3, HfO_2) and InP as substrate, using physics-based numerical modeling. Effects of body thickness downscaling to 2 nm, different gate oxides, and surface orientation [(100) and (111)] are examined by including all electron valleys and all relevant scattering mechanisms. We report that ultra-thin (111) Al_2O_3–InGaAs–InP devices offer greater electron mobility than (100) devices even in the extremely-thin channels. Furthermore, ultra-thin (100) InGaAs devices outperform SOI in terms of electron mobility for body thicknesses above ~4 nm, while (111) InGaAs channels are superior to SOI for all body thickness values above ~3 nm. The study of different gate oxides indicates that HfO_2 is the optimum gate dielectric regardless of device orientation, offering a mobility improvement of up to 124% for (111) and 149% for (100) surface orientation, when compared to the initial Al_2O_3–InGaAs–InP structure. The (111) orientation offers improvement over (100) device irrespective of the body thickness and gate oxide material, with the highest difference reported for SiO_2, followed by Al_2O_3 and HfO_2.

1. Introduction

$In_{0.53}Ga_{0.47}As$ is a promising channel material for future nMOSFETs since it provides high electron mobility and an acceptable bandgap [1]. Higher dielectric constant makes InGaAs devices more susceptible to short-channel effects (SCEs), which can be alleviated by employing ultra-thin-body (UTB) device architectures [2]. Different UTB InGaAs structures have been reported, ranging from InGaAs-on-insulator (InGaAs-OI) with body thicknesses (T_B) down to ~3 nm [3–5], over InGaAs FinFETs with relatively thick channels [6], to quantum-well FETs (QW FETs) where the InGaAs channel is sandwiched e.g. between InGaAs layers with lower Indium content [7]. The QW FETs based on InGaAs channel seem to be a promising device structure to replace silicon devices for the extremely-scaled CMOS nodes [8,9]. However, the advanced architectures regularly cause a strong mobility deterioration in ultra-thin channels, which degrades transistor performance. For example, Yokoyama et al. [10] demonstrated mobility reduction from ~1000 $cm^2/V\,s$ down to ~10 $cm^2/V\,s$ when T_B is scaled down from 9 nm to 3.5 nm in InGaAs-OI MOSFETs. Recently, Alian et al. [11] reported higher electron mobility data ranging from 3000 $cm^2/V\,s$ for T_B = 15 nm down to 110 $cm^2/V\,s$ for the 3 nm-thick InGaAs device. Furthermore, previous theoretical studies have shown that (100)-oriented UTB InGaAs channels outperform SOI devices only above certain body thickness (around ~5 nm) due to strong surface roughness and thickness-fluctuation-induced scattering caused by the low interface quality [12].

Therefore, the strong mobility decrease in UTBs demands an approach for mobility improvement in sub-5 nm-thick InGaAs layers. One among the possible methods is using alternative surface orientations, e.g. Ishii et al. [13] have shown that (111)-oriented bulk InGaAs channels offer up to 30% improved electron mobility compared to (100) device. However, experimental data is available only for bulk (111) InGaAs MOSFET and virtually nothing is known about electron mobility in UTB (111)-oriented InGaAs devices [14]. Therefore, a modeling study is necessary in order to determine the behavior of mobility in ultra-thin (111) InGaAs channels. Furthermore, the devices from [13] are fabricated with Al_2O_3 as gate dielectric, which necessitates the assessment of the impact of other technologically relevant gate oxides on the mobility in UTB InGaAs devices. In this paper, we use physics-based modeling to study the impact of body thickness downscaling, (111) and (100) surface orientation, and different gate oxides (SiO_2, Al_2O_3, and HfO_2), on the electron mobility in ultra-thin InGaAs layers sandwiched between a gate oxide and InP as substrate. We found that the advantage of (111) surface reported for bulk InGaAs devices is preserved in

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UTB architectures, and that using different gate oxides could lead to significant mobility improvements as well.

2. Mobility modeling

The Schrödinger–Poisson system is solved self-consistently in order to find the eigenstates in the InGaAs channel that is sandwiched between 12 nm-thick gate oxide and InP as bottom substrate. This structure is chosen to match the fabricated devices from [13], since that report contains the measured mobility data for both (100) and (111) bulk Al_2O_3–InGaAs–InP MOSFETs. The barrier heights are finite which results in wave-function penetration into the oxide and substrate. The electrons in Γ, Δ and L valley are included in the model in order to address the complex band-structure of InGaAs in mobility simulations. In addition, the band-structure effects in III–V UTBs are taken into account by employing T_B-dependent effective masses [12] and the following nonparabolicity factors $\alpha_\Gamma = 1.1$, $\alpha_\Delta = 0.55$, $\alpha_L = 0.44$. The calculation of the effective masses (confinement, conductivity and density-of-states effective mass) for (100) and (111) surface, and for all three valleys, is based on the rules for conduction-band constant-energy ellipsoids reported in [15], by assuming the transport direction (001) for the (100) surface orientation, and (112) direction for the (111) surface orientation.

Momentum relaxation time approximation (MRTA) is used to calculate the mobility for the 2DEG in the sub-20 nm-thick InGaAs channel [12,16]. Our model includes the following scattering mechanisms: non-polar acoustic and optical phonon (NPP), polar optical phonon (POP), and surface optical phonons (SOP) that must be considered when using high-k materials as gate dielectrics; surface roughness (SR) scattering using a Prange-Nee formula with wave-functions that penetrate into finite barriers which modifies the SR scattering both quantitatively and qualitatively (see discussion in Section 3.3). Coulomb scattering (CO) that covers ionized impurities (N_{II}) and interface charge (N_{int}); and scattering induced by alloy disorder (AD). The equations for all of the scattering rates can be found in [12] and references therein, except for SOP scattering. For the intra-valley scattering of electrons by SOPs, we use the approach proposed by Esseni et al. [17], but taking into account the contribution of only the front oxide layer that is a source of the SOP scattering potential. In contrast to [17], we use a simplified approach for SOP MRT where the coupled-MRT term is approximated with $(1-\cos\theta)$, where θ is the wave-vector redirection between the initial and final state, as is usually done for intra-subband transitions of e.g. SR MRT [18]. This approach is less computationally demanding, thus allowing the simulations of a large number of devices at about 10–15 bias points each.

The material and scattering parameters used in the simulations are listed in Table 1, while the SOP-related parameters are given in Table 2. The parameters L and Δ are the correlation length and amplitude of the surface roughness model, with subscripts B and F indicating the back and front interface, respectively. The parameter values for $In_{0.53}Ga_{0.47}As$ are taken directly (if available) or are linearly extrapolated from GaAs and InAs parameters available in the literature [19]. The total mobility is calculated using Kubo-Greenwood equation for subband mobilities, by summing up all the obtained subband mobilities weighted by corresponding subband inversion charge density [12].

Table 1
Material and scattering parameters used in self-consistent Schrödinger–Poisson and MRTA mobility simulations.

Material		GaAs	InAs
Bulk effective masses			
Valley	Γ	$m_l = m_t = 0.067$	$m_l = m_t = 0.023$
	Δ	$m_l = 1.90$, $m_t = 0.19$	$m_l = 1.90$, $m_t = 0.19$
	L	$m_l = 1.90$, $m_t = 0.075$	$m_l = 1.90$, $m_t = 0.075$
Bandstructure and scattering parameters			
$E_\Gamma = 0.75$ eV, $E_\Delta = 1.33$ eV, $E_L = 1.21$ eV			
$D_{AP,\Gamma} = 7$ eV, $D_{AP,\Delta} = 9.2$ eV, $D_{AP,L} = 9.0$ eV			
$E_{OP} = 32$ meV, $D_{OP} = 10 \times 10^8$ eV/cm			
$E_{POP} = 32$ meV, $\varepsilon_0 = 13.94$, $\varepsilon_\infty = 11.64$			
$v_{s,T} = 2974$ m/s, $v_{s,L} = 4253$ m/s, $\rho = 5506$ kg/m^3			
$a = 5.868$ Å, $V_0 = 0.8$ eV, $N_{II} = 10^{15}$ cm^{-3}			
InGaAs–InP (back) interface parameters			
$L_B = 2.0$ nm, $\Delta_B = 0.6$ nm, $N_{int,B} = 10^{11}$ cm^{-2}			
Al_2O_3–InGaAs (front) interface parameters			
(100)		$L_F = 2.0$ nm, $\Delta_F = 0.9$ nm	$N_{int,F} = 1.15 \times 10^{12}$ cm^{-2}
(111)		$L_F = 2.0$ nm, $\Delta_F = 0.7$ nm	$N_{int,F} = 9.45 \times 10^{11}$ cm^{-2}

Table 2
Parameters of polar phonons in dielectrics examined in this paper. Data is taken from [16].

Parameter	SiO_2	Al_2O_3	HfO_2
ε_0	3.9	12.53	22
ε_{int}	3.05	7.27	6.58
ε_∞	2.50	3.20	5.03
$\hbar\omega_{TO1}$ (meV)	55.60	48.18	12.40
$\hbar\omega_{TO2}$ (meV)	138.10	71.41	48.35

3. Simulation results and discussion

3.1. Model calibration on the Al_2O_3–InGaAs–InP structure

In the calibration simulations, the quality of the back (InGaAs–InP) interface is kept constant ($N_{int,B} = 10^{11}$ cm^{-2}, $L_B = 2.0$ nm, $\Delta_B = 0.6$ nm) while the parameters of the front (Al_2O_3–InGaAs) interface are fitted ($N_{int,F}, L_F, \Delta_F$) in order to achieve good match with the experimental data from [13]. Fig. 1 demonstrates good agreement between simulation and experiment for bulk Al_2O_3–InGaAs–InP MOSFETs, which demonstrates that all relevant scattering mechanisms and nonparabolicity effects are properly taken into account.

In the simulations, $T_B = 20$ nm was set for the bulk device even though the InGaAs thickness was 1 μm in the fabricated devices [13]. In Fig. 2, we have compared the potential profile and Γ-valley ground state wave-function for $T_B = 20$ nm and $T_B = 50$ nm to justify using a 20 nm-thick channel for the simulation and fitting of bulk mobility data. The comparison is done both in a relatively

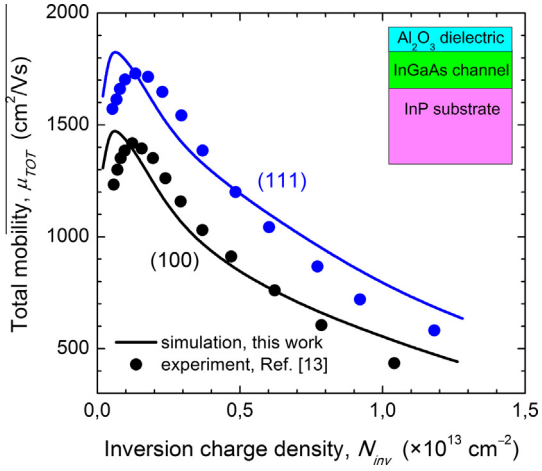

Fig. 1. Comparison between experimental and simulation data for (100) and (111) oriented bulk Al_2O_3–InGaAs–InP devices. Experimental data is taken from [13].

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