Available online at www.sciencedirect.com
SCIENCE DIRECT®
Solid-State Electronics 49 (2005) 1140–1152
SOLID-STATE ELECTRONICS
www.elsevier.com/locate/sse

Fowler–Nordheim high electric field stress of power VDMOSFETs

Goran S. Ristić [a,*], Momčilo M. Pejović [a], Aleksandar B. Jakšić [b]

[a] Faculty of Electronic Engineering, University of Niš, P.O. Box 73, 18001 Niš, Serbia
[b] Tyndall National Institute, Lee Maltings, Cork, Republic of Ireland

Received 18 October 2004; received in revised form 4 May 2005; accepted 8 May 2005

The review of this paper was arranged by Prof. S. Cristoloveanu

Abstract

The analysis of defect generations in SiO_2 and at SiO_2/Si interface during positive/negative high electric field stress of commercial n-channel power VDMOSFETs has been given. Some additional experiments containing the gate bias switching have helped in these defects nature investigations. The combined application of midgap subthreshold technique and charge pumping technique have represented very useful tool for the switching trap behavior revealing. The fixed trap density (ΔN_{ft}) and switching trap density (ΔN_{st}) in two power VDMOSFET types during Fowler–Nordheim injections have shown different behaviors.

PACS: 78.40.Fy; 73.40.Qv; 72.20.Ht; 72.20.Jv

Keywords: Fowler-Nordheim injection; High electric field stress; Oxide trapped charge; Interface traps; Switching traps; MOS transistor

1. Introduction

The existence of the defects in the gate oxide (SiO_2) and at gate oxide/substrate (SiO_2/Si) interface of the metal–oxide–semiconductor field-effect transistors (MOSFETs) is very important fact relating to their reliability [1–5]. The generation of positively/negatively charged defects has been observed in the oxide of metal–oxide–semiconductor (MOS) devices during several types of the experiments involving the passage of charge carriers through the oxide: avalanche hole injection, avalanche electron injection, high electric field stress, exposure to ionizing radiation and so on.

The aim of this paper is to investigate the behaviors of fixed traps and switching traps, formed by Fowler–Nordheim high electric field stress (F–N HEFS), in the commercial n-channel power VDMOSFETs (Vertical Double-Diffused MOSFETs), and to give the complete methodology for the experiments performing, and defects separation. The switching traps were divided into slow switching traps (border traps) and fast switching traps (true interface traps).

We have been performing very detailed investigations [6–9] (and references therein) concerning to the defect behaviors in commercial n-channel VDMOSFETs during both ionizing irradiation (IR) and thermal post-irradiation annealing, pushing us to investigate the HEFS effect on this transistor type, which has not been significantly investigated, although it could help in the defect behaviors understanding. Also, we have compared the effects of HEFS on two commercial n-channel power VDMOSFET types produced by different manufacturers.

* Corresponding author. Tel.: +381 18529324; fax: +381 18588399.
E-mail address: goranristic@elfak.ni.ac.yu (G.S. Ristić).

0038-1101/$ - see front matter © 2005 Elsevier Ltd. All rights reserved.
doi:10.1016/j.sse.2005.05.002

Nomenclature

List of symbols

C_{ox}	oxide capacitance per unit area (F/cm^2)
$\overline{D}_{it}$	average energetic interface trap density (cm^{-2}eV^{-1})
f	frequency (Hz)
k	Boltzman constant (eV/K)
L_{eff}	effective channel length (cm)
I_{cp}	substrate/charge pumping current (A)
I_D	drain-source current (A)
I_{MG}	midgap current (A)
$N_{A,D}$	channel doping (cm^{-3})
n_i	intrinsic carriers concentration (cm^{-3})
N_{it}	absolute interface trap density (cm^{-2})
q	absolute value of electron charge (C)
T	absolute temperature (K)
V_D	drain voltage (V)
V_{FB}^{cp}	charge pumping flatband voltage (V)
V_{FB}	flat band voltage (V)
V_G	gate voltage (V)
V_{MG0}	midgap voltage before stress (V)
V_{MG}	midgap voltage after stress (V)
V_T^{cp}	charge pumping threshold voltage (V)
V_{T0}	transistor threshold voltage before stress (V)
V_T	transistor threshold voltage after stress (V)
W	channel width (cm)
ΔE	energetic range (eV)
ΔN_{fst}	fast switching trap density (cm^{-2})
ΔN_{it}	interface trap density (cm^{-2})
ΔN_{ot}	net oxide trapped charge density (cm^{-2})
ΔN_{sst}	slow switching trap density (cm^{-2})
ΔN_{st}	switching trap density (cm^{-2})
ΔV_G	voltage amplitude (V)
ΔV_T	threshold voltage shift (V)
ϵ_s	silicon permittivity (F/cm)
Ψ_s	surface potential (V)
μ	transistor mobility (cm^{2}V^{-1}s^{-1})

List of abbreviations

CP	charge pumping
FST	fast switching traps
FT	fixed traps
HEFS	high electric field stress
IR	irradiation
IT	interface traps
MG	midgap-subthreshold
NCFT	negatively charged fixed traps
OTC	oxide trapped charge
PCFT	positively charged fixed traps
SEFA	switching electric field annealing
SHEFS	switching high electric field stress
SST	slow switching traps
ST	switching traps

2. Experimental details

The devices used in these experiments were two types of the commercial n-channel power VDMOSFETs: EFL1N10, manufactured by Ei-Microelectronics, Niš, and IRF510, manufactured by Intersil (formerly Harris Semiconductors). We had all data relating to EFL1N10 devices, manufactured in a standard, commercial process, with the the gate oxide nominal thickness of 100 nm. Also, we knew that IRF510 devices, encapsuled in plastic TO-220AB packages, were consisted of 1650 elementary hexagonal cells, and that they were also manufactured in a standard, commercial process, having an oxide thickness of 100 nm. We may only suppose that the similar technology processes were used for both device types.

The cross-section of two half-cell of the EFL1N10 transistors that consist of 860 hexagonal cells is shown in Fig. 1. The maximum voltage of these devices is 100 V, and maximum current is 1 A. The effective channel length is $L_{eff} = 2.6$ μm, and the channel width of a single cell is $W = 62.4$ μm. The starting material was 400 μm thick n-type Si wafers with (100) orientation, on which the n-epi layer of about 14 μm was grown. After implantation of the p^+-body region, the gate oxide with nominal thickness of 100 nm was grown in dry oxygen at 1100 °C, and annealed in nitrogen at 1100 °C for 20 min. There followed the deposition of 800 nm thick poly-Si gate, implantation of the p-channel and n^+-source regions, and deposition of 1 μm thick CVD oxide. After metallization and post-metallization anneal at 550 °C in nitrogen, devices were passivated and mounted in standard metal TO-39 packages.

Transistor subthreshold characteristics and transistor transfer characteristics, both in saturation, were measured using Keithley 2400 source-meter unit and Keithley 237 source measure unit, controlled by a PC. Using Keithley 2400 the DC voltage, changed in the steps of 0.05 V, in both the positive and negative gate voltage directions, was applied to the transistor gate, while using Keithley 237 the drain was biased with constant voltage $V_D = 10$ V (the source was grounded), and drain-source current I_D was measured in range from 10^{-11} to 10^{-1} A. The transistor threshold voltage before stress V_{T0}, as well as after stress V_T, were determined by the transfer characteristics in saturation, i.e. as the intersection between V_G-axis and the extrapolated linear region of the $(I_D)^{1/2}$–V_G curves, using the least square method performed by MATLAB program packet, which is modelled by the following equation [10]: