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Evolution of materials technology for stacked-capacitors in 65 nm embedded-DRAM

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Abstract

The architecture, materials choice and process technology for stacked-capacitors in embedded-DRAM applications are a crucial concern for each new technology node. An overview of the evolution of capacitor technology is presented from the early days of planar PIS (poly/insulator/silicon) capacitors to the MIM (metal/insulator/metal) capacitors used for todays 65 nm technology node. In comparing Ta_2O_5, HfO_2 and Al_2O_3 as high-*k* dielectric for use in 65 nm eDRAM technology, Al_2O_3 is found to give a good compromise between capacitor performance and manufacturability. The use of atomic layer deposition (ALD) is identified to be an enabling technology for both high-*k* dielectrics and capacitor electrodes.
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Keywords: DRAM; Capacitor; MIM; High-*k*; Dielectric; Electrode; Atomic layer deposition, ALD

1. Introduction

A typical DRAM cell consists of an access transistor and a storage capacitor (1T/1C). There are two types of storage capacitors, stacked-capacitors and trench capacitors, of which the latter offers highest density, at the expense of process complexity [1].

Trench capacitors are less suitable for integration of high-*k* dielectrics because they are formed before the transistors with their associated high temperature anneals.

For embedded-DRAM (eDRAM) we have adopted stacked capacitors as being the most cost-competitive solution. Because stacked capacitors are formed after the transistors the overall impact on performance of the CMOS core process is of primary concern.

If the thermal budget of the capacitor processing is too high, it will degrade transistor performance.

In the first part of this paper, we will outline the general evolution of capacitor architectures.

Next we will detail how capacitor materials and processing have evolved from furnace-based polysilicon electrodes with (oxy)nitride dielectrics towards metallic electrodes with high-*k* dielectrics, both processed by atomic layer deposition (ALD) at moderate thermal budget, favourable to eDRAM applications.

2. Capacitor architecture evolution

Technical innovation in capacitor processing continued over the past 20 years in the industry, enabling DRAM

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scaling into the sub-100 nm regime of today. Fig. 1 illustrates the successive architectures adopted. In the following summary of DRAM capacitor technology since 1982, no distinction is made between stand-alone and eDRAM as both are driven by similar concerns like high capacitance, high breakdown voltage and high capacitor density.

Between 1982 and 1985, DRAM density increased from 64 Kb to 1 Mb [2] using planar 2D-capacitors, from the early PIS structure (poly–insulator–silicon: Fig. 1a) with gate oxide dielectric to PIP capacitors (poly–insulator–poly: Fig. 1b) which allow adjustment of dielectric thickness and capacitance. The stacked capacitor, first proposed in 1978 by Koyanagi et al. [3], was applied for industrial 1 Mb integration in 1985 [4], using a triple poly (Fig. 1c and d).

From 1986 to 1990, DRAM density is driven from 1 to 16 Mb with design rules ranging from 0.8 to 0.4 μm. These cells are produced with 3D-architectures and SiO_2/Si_3N_4 dielectrics (ON/ONO). The capacitor surface is extended in the third dimension.

From 1991 to 2000, DRAM evolution went from 64 Mb towards the Gigabit era. Starting with a 0.4 μm CMOS process using a stacked-capacitor cell, 1 Gb is demonstrated with 0.25–0.16 μm CMOS. The third dimension is no longer sufficient to maintain a large capacitance density (in terms of fF/μm^2). Thus the Si_3N_4 content is optimized to provide high capacitance and low leakage in 3D-PIP architectures. Furthermore, the dielectric process is focused on low thermal budget to ensure compatibility with CMOS platforms.

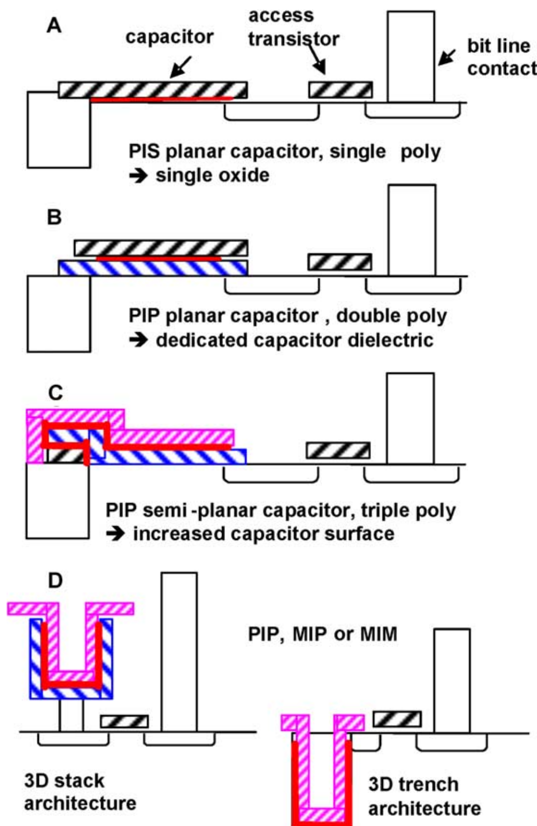

Fig. 1. DRAM architecture evolution from 1980 to 2005.

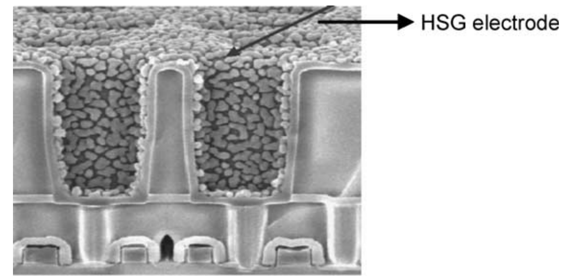

Fig. 2. HSG bottom electrode in 120 nm e-DRAM technology.

Hemi-spherical grained polysilicon (HSG) is introduced as bottom-electrode in the 0.18 and 0.15 μm nodes [5], increasing the effective surface, as illustrated in Fig. 2.

Next efforts were focused on improving data-rate rather than bit density and especially on embedded applications with a pure Si_3N_4 dielectric.

From 2001 onwards, radical dielectric material changes appear. Si_3N_4 is abandoned due to its high thermal budget. MIS stacked-capacitors using high-*k* dielectrics and metallic top electrodes are reported with 1 Gb chips using Ta_2O_5 [6] and 4 Gb using Al_2O_3 [7] in 0.10 μm technology. TiN is the mainstream electrode material whereas alternatives, like WN [8] or Ru [9], are being studied for higher workfunction and oxidation resistance.

DRAM then enters into the sub-100 nm technology CMOS nodes, focusing on design and application issues. New high-*k* dielectric materials, with low thermal budget, are introduced to replace Ta_2O_5, along with the introduction of MIM capacitors.

Fig. 3 summarizes the evolution of DRAM density, technology node, capacitor structure and dielectrics.

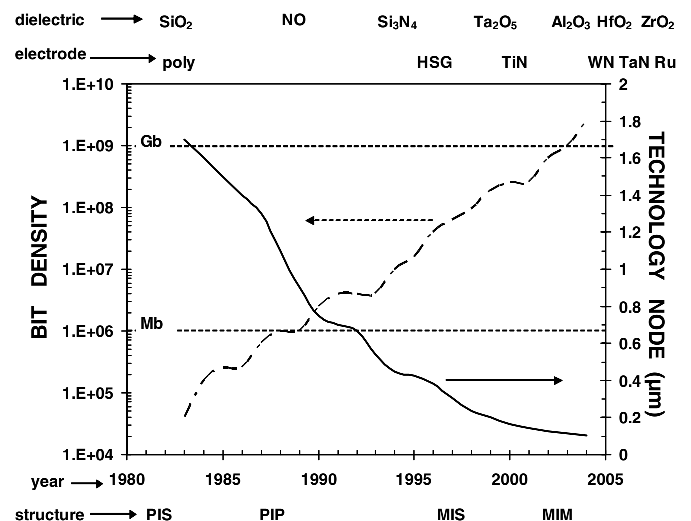

Fig. 3. Trend of DRAM production node, bit density, dielectrics and electrode materials.

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