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A comprehensive study of carrier velocity modulation in DGSOI transistors

C. Sampedro [a,*], F. Gámiz [a], A. Godoy [a], M. Prunnila [b], J. Ahopelto [b]

[a] Departamento de Electrónica, Universidad de Granada, 18071 Granada, Spain
[b] VTT Information Technology, P.O. Box 1208, FIN-02044 Espoo, Finland

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Abstract

Velocity modulation transistors (VMT) are proposed as a way to explode short transit time between two adjacent channels with different transport properties in order to obtain a fast switch. Originally proposed for III–V heterostructures, a Monte Carlo study of silicon-based VMTs is presented in this work showing that surface roughness in double-gate silicon-on-insulator devices can be used as a mobility degradation mechanism to obtain current ratios higher than 30 and therefore feasible devices. Transient simulations have been also carried out obtaining sub-picosecond switch times for 0.1 μm gate length. Switch time limitations are also discussed including both intrinsic and extrinsic factors.

Keywords: Velocity modulation transistor; Double gate SOI; Monte carlo

1. Introduction

In conventional field effect transistors (FET) the switching time is controlled by changing the carrier concentration in the channel, and therefore by the transit time of the carriers from source to drain [1]. As a consequence, the transistor channel length should be reduced well below 100 nm in order to obtain transit times in the sub-picosecond range, and as a consequence, frequencies of operation in the terahertz range [2,3]. However, in order to control the negative short channel effects (SCE) in those channel lengths double-gated silicon on insulator devices (DGSOI) can be used, but it is still needed very expensive and advanced facilities, and sometimes still unknown technological solutions for mass production [4]. An original proposal to reduce the switching time was introduced by Sakaki in 1982 [5]. The concept of velocity modulation transistor (VMT) explodes the perpendicular transit time between two adjacent channels of very different transport properties. The essential requirements for velocity modulation are twofold: (1) To switch the electron gas between two channels without changing the carrier density and (2) to create large enough mobility difference between both interfaces.

This device was originally proposed using III–V heterostructures such as *n*-AlGaAs/GaAs/*n*-AlGaAs forming two different channels at the heterointerfaces in GaAs [5]. One of the channels was highly doped with compensated donor and acceptor dopants, whereas the other one was kept undoped. In that case the compensated-doped channel formed the low mobility channel and the undoped one the high mobility channel. Several works can be found in the literature based on different heterostructures [6] using the same procedure to obtain differences on the transport properties. Current ratios obtained for those cases were smaller than 3 while a practical device should present, at least, a ratio of 10.

* Corresponding author. Tel.: +34 958 240490; fax: +34 958 243230.
E-mail address: csampe@ugr.es (C. Sampedro).

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Obviously, it would be very interesting to realize this idea on a silicon-based technology since it could be operated in the "teraherz gap" with applications on health and security equipment. Thanks to the flexibility of silicon-on-insulator (SOI) technology nowadays is possible to create such heterostructures in silicon-based devices [7]. A first performance prediction study of a VMT-like structure in Si was described in [8] where the degradation mechanism for the low mobility channel was again a compensated doping profile. Due to the fact that in this approach, front and back gate lengths were different a high electron density modulation was present (higher than 25%) between the two conduction states leading to a non-proper operation as VMT (again the achieved current ratio was approximately 3). Moreover, very recent experimental studies report that it is possible to move charge from the top interface to the bottom one in DGSOI devices obtaining velocity modulation at room temperature keeping constant the actual inversion charge constant [9]. So that, the aim of this work is to carry out a thorough investigation about the performance of DGSOI transistors operated as VMT at room temperature considering surface roughness instead doping compensation as a degradation mechanism to create a low mobility channel.

The outline of this paper is as follows. Section 2 describes the structure and operation conditions for the DGSOI used to simulate velocity modulation in silicon-based devices. The ensemble Monte Carlo (EMC) simulator used in this work is described in Section 3. Section 4 shows the results obtained from the simulations for both stationary and transient operation. Extrinsic and intrinsic switch time limitations are commented in Section 5. Finally the main conclusions obtained in this work are drawn in Section 6.

2. Description of a DGSOI transistor operated as a VMT

The structure under study in this work is a DGSOI transistor with a silicon channel thickness of $T_W = 20$ nm, gate length of $L_G = 100$ nm and oxide thickness of $T_{ox} = 10$ nm for both front and back gates. Source and drain have a doping concentration of $N_D = 10^{19}$ cm^{-3} and the channel is lightly doped ($N_A = 10^{12}$ cm^{-3}). The device under study is depicted in Fig. 1.

VMT operation demands two channels with different transport properties. As has been mentioned before, high doping has been used normally as degradation mechanism in order to increase Coulomb scattering in the low mobility channel. The drawback of this mechanism is that Coulomb scattering affects also the mobility in the other channel reducing the mobility ratio and therefore the performance of the device. Therefore, it becomes necessary to choose a degradation mechanism

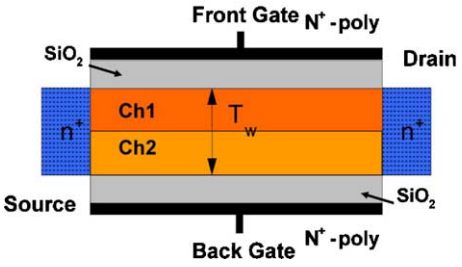

Fig. 1. DGSOI structure proposed to be operated as VMT.

which degrades the transport properties only in one of the channels (i.e. near to one of the interfaces). Pros and cons of different degradation mechanisms such as Coulomb scattering, the use of an amorphous material or the creation of an intentionally rough interface have been analyzed in [10]. Fig. 2 shows 1D Poisson–Schrödinger Monte Carlo simulations of the electron mobility in front and back channels for the DGSOI structure under study where one of the interfaces is very rough (the surface roughness parameters provided by experimental measurements were $\Delta_{sr} = 2$ nm, $L_{sr} = 15$ nm). The simulator has been described elsewhere [11,12].

As can be observed, μ_n in the degraded channel is very low in the whole range of inversion charge concentration and the mobility in the other channel is also affected by the surface roughness, specially at low inversion charge concentrations. However, for electron densities of 5×10^{12} cm^{-2} and higher, this influence is reduced and a ratio among the mobilities in both channels (μ_A/μ_B) higher than 30 is achieved. An intentionally degraded Si–SiO$_2$ interface will be used for the following study mainly for two reasons: (1) The mobility ratio obtained produces a higher current ratio than when Coulomb scattering is used as main degradation mechanism. (2) From a technological point of view a highly

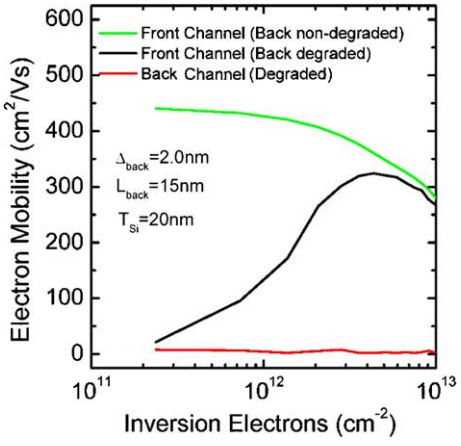

Fig. 2. Electron mobility in the front channel (middle curve) and in the back channel (lowest curve) for a degraded back interface by a rough back interface.