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Letter

High performance, foldable, organic memories based on ultra-low voltage, thin film transistors

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ABSTRACT

We report on the fabrication of highly flexible OTFT-based memory elements with excellent mechanical stability and high retention time. The devices have been fabricated using a combination of two ultrathin AlOx and Parylene C as dielectric, and TIPS-Pentacene as the semiconductor, obtaining high performing low voltage transistors with mobility up to 0.4 $cm^2/V\,s$, and I_{on}/I_{off} ratio of 10^5. Charge trapping in the Parylene C electret layer is the mechanism that allows employing these devices as non volatile memory elements, with retention time as high as 4×10^5 s. The electromechanical characterization demonstrated that such memory elements can be cyclically bent around a cylinder with a radius of 150 μm without losing the stored data.

1. Introduction

The possibility of developing fully functional organic electronic circuits is critically dependent on the ability to realize a full set of electronic functionalities based on organic devices. So far, huge steps forward have been done towards the realization of these objectives. In particular, low voltage, fast switching transistors have already been demonstrated [1–4], a whole set of electronic sensing elements has already been developed [5–8], not to mention organic solar cells for energy storage and organic LED for displays. However, to complete the scene, a fundamental function is still missing, i.e. reliable data storage. Over the past few years, considerable effort has been spent on the development and optimization of memory elements based on organic polymers. Memory elements should possibly be non-volatile (data must be retained when power is switched off); in addition, they must be programmed, erased, read, at low voltages and in a reasonably short time. Scientists investigated several possible strategies that may be grouped into two big categories: (i) 2-terminals devices based on resistive switching (i.e. a bistable electrical behavior between 2 different resistive states); (ii) transistor-based memories. The first category unfortunately suffers a strong limitation: when memory elements are arranged into an array structure, for instance in a crossbar configuration, cross talking between adjacent elements can strongly affect the single device behavior; as a consequence, this approach typically requires the coupling of a single memory element with a series diode [9].

On the contrary, in a transistor-based memory element, storage is coupled with the switching ability of the transistor, thus strongly reducing the electrical cross talking between adjacent elements in an array configuration. These memory elements can be fabricated with different structures. For instance, there are memories based on the use of ferroelectric materials, such as poly[(vinylidenefluoride-co-trifluoroethylene] (P(VDF-TrFE)), for the fabrication of the gate dielectric. In this case, the memory function is obtained through the reversible polarization of the dielectric [10,11]. However, this solution has several

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limits, in particular, the coercive voltage required to reverse the dielectric polarization of the ferroelectric material increases with film thickness, thus strongly limiting the bias operating window of the device. Alternatively, as proposed by Sekitani et al. [12], it is possible to employ a floating gate transistor based on an organic device similarly to what has already been demonstrated with silicon. However, similar structures require a considerable effort in optimizing the device architecture. Other possibilities include the employment of metal nanoparticles embedded into the active channel to obtain charge trapping sites within the organic semiconductor [13–15]. Charge is trapped by applying a certain bias to the device in the writing step, and is de-trapped in the erasing step. Again, the fabrication of such structures is quite critical in term of simplicity and reproducibility.

Finally, another interesting approach consists in the employment of a combination of a low-k dielectric (called electret) and a high-k (blocking) insulator. The memory element is written when a charge is trapped at the boundary between the two dielectric layers and canceled when the charge is de-trapped back into the device channel. The blocking layer is generally required to avoid charges trapped in the electret to move further towards the gate electrode during device operation [16–18]. Moreover, in order to fully exploit the main advantages of devices based on organic semiconductors, it would also be important to develop such structures onto flexible substrate and demonstrate that they are able to sustain continuous mechanical deformation. Several examples have been reported in this sense. For instance Ji et al. [19] reported about the fabrication of flexible arrays of resistive memory devices capable to be bent down to 3 mm without compromising their functionality. Other works [20,21] reported about flexible (high voltage) OTFT-based memory elements but in both cases the devices have been tested only with bending radii not smaller than 6 mm and 20 mm respectively. A significant improvement in terms of mechanical stability was recently reported by Kim et al. [22]. They have fabricated high performing OTFT-based memory elements operating at sub-millimeter bending radii. However, these devices, based on the employment of a ferroelectric polymer, require high operating voltages, and have been tested for bending radii not smaller than 0.5 mm.

In this paper we report about the employment of a hybrid combination of two ultrathin gate dielectrics for the realization of low voltage transistors-based memory elements. We demonstrated that these devices can be operated in air with retention times higher than 10^5 s. Moreover, we also tested their mechanical stability to bending radii as small as 150 μm. Very interestingly, we observed that the reported devices are characterized by a remarkable mechanical stability, and can be cyclically deformed at such a small bending radius for more than 1000 cycles without a significant variation of their electrical performances.

2. Materials and methods

The devices have been fabricated onto different plastic substrates, namely a 175 μm thick polyethylene terephthalate (PET), and 13 μm thick Kapton® films. In all cases, the first step consisted in the deposition of an aluminum film (nominal thickness 80 nm) that acts as the gate electrode. A 6 nm thick aluminum oxide film has been subsequently grown on the top the gate electrode by exposing its surface to UV-ozone treatment according to the procedure reported in [3]. A second ultrathin insulating film was then deposited in order to increase on one hand the vertical resistance of the dielectric layer, and, on the other hand, to create a dielectric interface where the charges can be injected and trapped. In the reported devices, a 40 nm-thick Parylene C film was deposited by Chemical Vapor Deposition (CVD) (see Fig. 1a and b). The final steps consisted in the deposition of gold source and drain electrodes, patterned by means of standard photolithography, and in the deposition of the organic active layer. In all cases, 6,13-Bis(triisopropylsilylethynyl)pentacene (TIPS Pentacene) was employed as organic semiconductor, and was deposited from liquid phase (0.5% in weight in toluene) by drop casting. After deposition, the substrate has been annealed for 30 min at 90 °C in order to remove any residual solvent and to improve the crystallinity of the film. All the electrical measurements have been performed in ambient atmosphere in dark using a HP4155A and Keithley 2636 source-meter.

3. Results and discussion

Thanks to the high capacitance of the gate dielectric, due to the very small thickness of the employed gate dielectrics, the devices can be operated at voltages as low as 2 V showing remarkably good performances. In particular, charge carrier mobility up to 0.4 $cm^2/V\,s$, threshold voltages usually ranging around −0.2/−0.4 V and I_{on}/I_{off} ratio up to 10^5 (see Fig. 1c) were recorded; moreover, an average quasi-static breakdown field of about 3 MV/cm was measured on more than 20 devices.

In order to characterize the devices as memory elements, we have applied single negative V_{GS} pulses (in the following, we will call these negative pulses V_{prog}), of the duration of 10 ms, keeping V_{DS} at 0 V. In particular, we applied V_{GS} pulses of different amplitudes, from −5 V up to −25 V. Interestingly, we have observed that in all cases, a negative V_{prog} always induces a shift of the transistor threshold voltage towards more negative values. However, some marked differences have been observed with different V_{prog} values.

For V_{prog} values between 0 and −10 V, we observed very small threshold voltage shifts, in the range of −0.3/−0.4 V, and most importantly, this parameter was restored to its previous value within a very small period of time (30 min). Increasing the pulse amplitude up to −15 V (see Fig. 2), a much more pronounced shift of the threshold voltage was induced. In this case, we observed an average threshold voltage shift close to −1 V and, typically, the retention time exceeds the value of 2×10^4 s (5 h).

Interestingly, when positive V_{prog} pulses of the same amplitudes are applied to a freshly made device (never programmed before), no significant shift of the threshold voltage has ever been observed.