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Organic field-effect transistor circuits using atomic layer deposited gate dielectrics patterned by reverse stamping

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ABSTRACT

We report on a reverse stamping method to produce via-holes in circuits comprising acene-based top-gate organic field-effect transistors (OFETs) having a CYTOP/Al_2O_3 (by atomic layer deposition) bilayer gate dielectric. This method relies on the weak adhesive force that exists between a small molecule acene film and a polymer to enable easy delamination of the bilayer gate dielectric by using a PDMS stamp. We demonstrate the effectiveness of this method by fabricating simple circuits using top-gate triisopropylsilylethynyl pentacene (TIPS-pentacene)/poly (triarylamine) (PTAA) OFETs.

1. Introduction

Organic field-effect transistors (OFETs) continue to mature into an appealing technology for a wide variety of commercial applications. Noticeable progress has been reported by many researchers in recent years. Carrier mobility values reported in OFETs now reach values that are at least one order of magnitude larger [1] than mobility values reported on amorphous silicon transistors [2]. The threshold voltage values have also decreased to meet low voltage driving requirements [3]. In addition to achieving high electrical performance, the operational and environmental stability of OFETs has also improved significantly [4–6]. Progress in discrete OFET performance has led to development and improvement of integrated OFET circuits, such as a clocked sequential complementary circuit [7], an 8-bit microprocessor [8], user customizable logic paper [9], and a braille display [10] among others, showing the potential of OFETs to lead to a new generation of flexible electronics.

OFETs need to be fabricated by scalable, low-cost manufacturing processes for this technology to reach the market. Realization of solution-processed discrete OFETs is the first step towards developing a scalable technology with low fabrication cost. To date, electrodes, gate dielectric layers and semiconductors have all been processed from solution [5,11,12] and patterned using techniques such as soft lithography [13], selective physical delamination [14,15], and printing [11]. However, the realization of integrated circuits and systems using low-cost methods for patterning via-holes, essential for vertical interconnections between upper and lower electrodes, has received relatively less attention in the literature. Most reports of OFET circuits with high levels of performance and integration have relied on techniques commonly used in the microelectronic industry, such as photolithography and chemical etchings or chemical lift-off processes to make via-holes [16]. However, fewer reports on alternative patterning approaches exist such as dissolution of polymeric dielectric layers by

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locally printing a solvent [17–19], deposition of noble metals to selectively define areas where the growth of self-assembled monolayers (SAM) is hindered [3], and direct patterning by printing polymeric dielectric films [5]. However, these alternative approaches share a common limitation in that they are not capable of patterning inorganic layers, in particular, high-quality metal-oxide layers deposited by atomic layer deposition (ALD).

ALD is an important technique for the development of printed electronic applications because it has already been shown to lead to thin films with unique environmental barrier properties [20,21]. This is because the ALD method uses self-limiting surface reactions to allow controlled layer-by-layer growth of uniform and highly-conformal films [22]. Furthermore, ALD technology is making headways into becoming a widespread industrial technique as evidenced by recent developments in high-speed or spatial ALD processes, which allow high deposition rates (larger than 1.2 nm/s [23]) and are compatible with roll-to-roll fabrication methods.

ALD-grown metal–oxide films have been typically used as gate dielectrics in bottom-gate OFET geometries showing high-performance and low-voltage operation; both, in discrete devices [24] and circuits [25]. Recently, we have shown that top-gate OFETs, with a CYTOP/Al_2O_3(by ALD) bilayer gate dielectric, display high environmental and operational stability in air [4] and in water [26]; making their use as reusable chemical and biological sensors in aqueous solutions possible [27]. However, the use of ALD layers as gate dielectrics in top-gate OFET geometries presents a further challenge in that existing methods for patterning via-holes require harsh photolithographic methods [28] or selective area ALD, via the deposition of blocking layers or inhibitors [29–31], which are not compatible with top-gate OFET fabrication methods. Hence, a need exists to develop alternative methods to pattern ALD-synthesized films used in electronic devices.

In this work, we report on a reverse stamping method that allows easy patterning of ALD-synthesized films, and in particular, the realization of via-holes in top-gate triisopropylsilylethynyl pentacene (TIPS-pentacene)/poly (triarylamine) (PTAA) OFET circuits. In contrast with additive soft lithography, wherein a stamp is used to add up a patterned material or film to a substrate, the reverse stamping method removes a targeted area of a film off the substrate. This dry patterning method does not require vacuum-process steps or chemical etching and can be generally applied to OFET structures with high dielectric constant inorganic insulators. Here, we demonstrate the successful application of this method by fabricating top-gate OFET-based electronic circuits: inverters, NOR2 gates, ring oscillators, and 2-to-4 decoder circuits.

2. Experimental

As a test platform for the reverse stamping method, bottom-contact top-gate TIPS-pentacene transistors were fabricated as follows: Ti/Au (6/70 nm) was deposited on the cleaned glass substrate (Corning® Eagle$^{2000™}$) by a Denton e-beam evaporator at a deposition rate of 1 Å/s (Ti) and 1 Å/s (Au) under 2×10^{-6} Torr at room temperature for the source/drain electrodes of the organic transistors and metal lines of circuits with shadow masks. In order to improve contact properties between source/drain electrodes and TIPS-pentacene, the substrates were immersed into 10 mM pentafluorobenzenethiol (PFBT) solution in ethanol for 15 min and rinsed with pure ethanol for 1 min followed by 5 min of annealing on a hot plate at 60 °C. A 1:1 weight ratio of TIPS-pentacene (15 mg) and PTAA (15 mg) blend was dissolved in 1,2,3,4-tetrahydronaphtalene anhydrous for a concentration of 30 mg/mL. A 70 nm-thick TIPS-pentacene layer was formed by spin-coating this solution at 500 rpm for 10 s with 500 rpm/s acceleration and 2000 rpm for 20 s with 1000 rpm/s acceleration, followed by annealing at 100 °C for 15 min on a hot plate in a N_2-filled glove box. CYTOP (ASAHI GLASS, CTL-890 M) diluted with a solvent (ASAHI GLASS, CT-SOLV180) (1:3.5 volume ratio) was spin-coated on top of the semiconductor layer at 3000 rpm for 60 s (acceleration of 10,000 rpm/s) to produce a 35 nm thick film. Samples were annealed at 100 °C for 10 min on a hot plate inside the glove box. A 40 nm-thick Al_2O_3 film was grown in a Savannah 100 ALD system from Cambridge Nanotech. The film was deposited at a processing temperature of 110 °C using alternating exposures of trimethylaluminum ($Al(CH_3)_3$) and water vapor as these deposition conditions have been proved to enable excellent barrier properties of Al_2O_3 films in previous reports [4,27].

Before the deposition of a gate metal, a reverse stamping step was performed in order to make vertical interconnections (via-holes) between lower gold and upper silver electrodes. A poly(dimethylsiloxane) (PDMS) stamp with embossed patterns at the position of the via-holes was fabricated as follows: the base was first mixed with the agent (Gelest OE™ 41) in a weight ratio of 1:1 and the solution was then gently poured onto the pre-defined mold made of glass without trapped air bubbles in it. The pre-defined mold was then transferred to an oven for curing at 80 °C for 1hour under atmospheric pressure and then cooled down before the PDMS stamp was peeled off from the mold. The embossed PDMS stamp was aligned with the OFET substrate, softly pressed onto the CYTOP/Al_2O_3 bilayer surface and peeled-off from the substrate to define the via-holes. The reverse stamping method was characterized by spectroscopic ellipsometry studies (J.A. Woollam M-2000UI) on samples comprising the dielectrics and semiconductor layers on glass. The optical properties of all layers and their thickness values were derived by modeling of spectroscopic ellipsometry data acquired at three angles of incidence: 65°, 70° and 75°, on samples before and after reverse stamping.

The transistor gate electrode and circuit interconnections were fabricated by depositing a 100 nm-thick silver layer through a shadow mask using a thermal evaporator at a base pressure of $<5 \times 10^{-7}$ Torr.

A 7-stage ring oscillator and a 2-to-4 decoder circuit composed of four NOR2 gates were designed by Cadence Virtuoso Schematic Editor and Layout Suite and its performance simulated by Synopsys HSPICE prior to the fabrication. The inverters and NOR2 gates consist of only p-type transistors so that a pseudo complementary design was adapted [32]. In the design, via-holes clustered at